High Efficiency 1.5MHz 2A Synchronous Step Down Converter

1 Features

- Input Voltage Range: 2.7V to 5.75V
- Output Voltage Range: 0.6V to V_{IN}
- 2A Constant Output Current
- 0.6V Reference Voltage
- Integrated 65mΩ / 60mΩ MOSFETs
- 35uA Quiescent Current
- 1.5MHz Switching Frequency
- Internal 0.7ms Soft-Start Time
- Internal Compensation Function
- 100% Dropout Operation
- Input Over Voltage Protection
- Over Current Protection
- Hiccup Short Circuit Protection
- Over Temperature Protection
- RoHS Compliant and Halogen-Free

2 Applications

- Set-Top Box
- LCD TV & Table
- AP Router & Wi-Fi
- G-PON, E-PON, xDSL

3 Description

The SC1104 is a high efficiency, high frequency synchronous DC/DC step-down converter. The 100% duty cycle feature provides low dropout operation, extending battery life in portable systems.

The internal synchronous switch increases efficiency and eliminates the need for external schottky diode. At shutdown mode, the input supply current is less than 1μA.

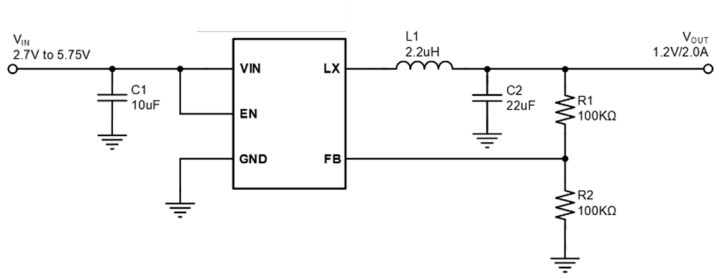
The SC1104 fault protection includes over current protection, short circuit protection, under voltage lockout protection and thermal shutdown. The Internal soft-start function prevents inrush current at turn-on. The SC1104 is offered in a SOT23-5 package.

Device Information[1]

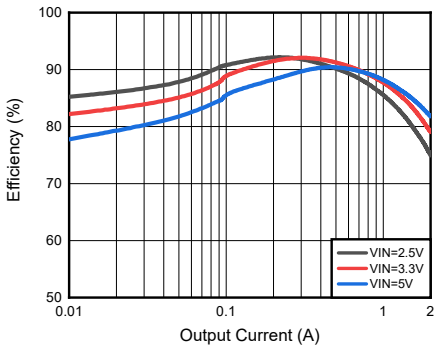
PART NUMBER	PACKAGE	BODY SIZE (NOM)
SC1104	SOT23-5	2.90mm x 2.90mm

1. For packaging details, see *Package Information* section.

Simplified Application Schematic



1.2V Output Efficiency



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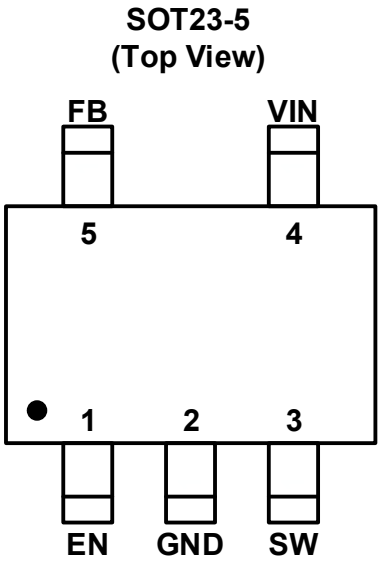
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN NUMBER		PIN TYPE[1]	FUNCTION
NAME	NUM		
EN	1	I	Enable control pin. Pull high enables the device, and pull low to disables the device and turns it into shutdown. Don't leave this pin floating.
GND	2	G	Ground pin.
SW	3	P	Power switching node. Connect an inductor to the drains of internal high side PMOS and low side NMOS.
VIN	4	P	Power supply input pin. Placed input capacitors as close as possible from VIN to GND to avoid noise influence.
FB	5	I	Feedback pin for the internal control loop. Connect this pin to the external feedback divider.

1. I = input, P = power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	7.0	V
V_{SW}	Switching node voltage (SW)	–0.3	V_{IN}+0.3	V
V_{IO}	I/O pin voltage (EN, FB)	–0.3	V_{IN}	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C
P_{max}	SOT23-5 Maximum power dissipation @ T_A=+25°C		0.4	W

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	2.7		5.75	V
V_{OUT}	Output voltage	0.6		V_{IN}	V
I_{OUT}	Output current	0		2	A
T_J	Operating junction temperature	-40		125	°C

1. The device is not guaranteed to function outside of its operating conditions.
2. Refer to the *Application Information* section for further information.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Natural convection, 2S2P PCB	SOT23-5	117.71	°C/W
Θ_{JB}	Cold plate, 2S2P PCB	SOT23-5	59.55	°C/W
Θ_{JC}	Cold plate, 2S2P PCB	SOT23-5	34.00	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	SOT23-5	59.46	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	SOT23-5	2.27	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_{IN} = V_{EN} = 5V, T_J = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
$V_{IN(OVP)}$	Input overvoltage protection			6.1		V
I_Q	Quiescent current	No switching		35		μA
I_{SHDN}	Shutdown current	EN = 0V		0.1	1	μA
V_{UVLO}	Under voltage lockout	V_{IN} rising	1.5	2.0	2.5	V
V_{UVLO_HYS}	Under voltage lockout hysteresis			200		mV
ENABLE						
V_{EN_RISE}	Rising enable threshold	2.7V ≤ V_{IN} ≤ 5.75V		1.3	1.5	V
V_{EN_FALL}	Falling enable threshold	2.7V ≤ V_{IN} ≤ 5.75V	0.4	0.9		V
I_{EN}	EN input current	V_{EN} = 2V		0.1	1	uA
VOLTAGE REFERENCE						
V_{FB}	Feedback voltage	V_{IN} = 2.7 to 5.75V	0.588	0.6	0.612	V
I_{FB}	Feedback leakage current	V_{FB} = V_{IN}		0.01	1	uA
t_{ss}	Soft startup time			0.7		ms
INTEGRATED POWER MOSFETS						
$R_{DS(on)}$	High-side FET on resistance			65		mΩ
	Low-side FET on resistance			60		mΩ
SWITCHING REGULATOR						
F_{SW}	Switching frequency	I_{OUT} = 1.0A		1.5		MHz
D_{MAX}	Maximum duty cycle				100	%
T_{MIN}	Minimum on time[1]			50		nS
R_{DISCHG}	Output discharge resistance			1		KΩ
CURRENT LIMIT						
I_{LIM}	High-side current limit[1]			4.0		A

Electrical Characteristics(continued)

V_{IN} = V_{EN} = 5V, T_J = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWM						
T_{TSD}	Thermal shutdown temperature[1]			160		°C
T_{HYS}	Thermal shutdown hysteresis[1]			25		°C

1. Guaranteed by design and engineering sample characterization.

5.6 Typical Characteristics

T_A = -40°C to 125°C, unless otherwise noted.

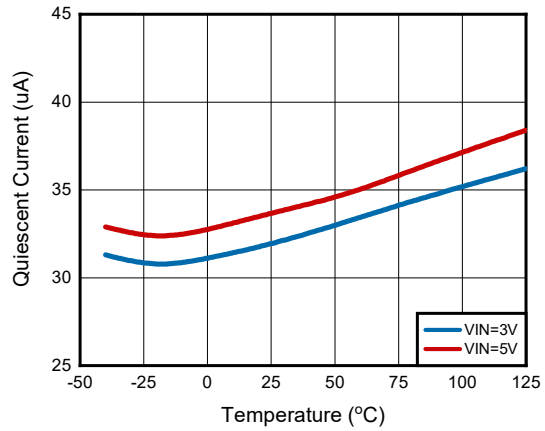


Figure 1. Quiescent Current vs. Temperature

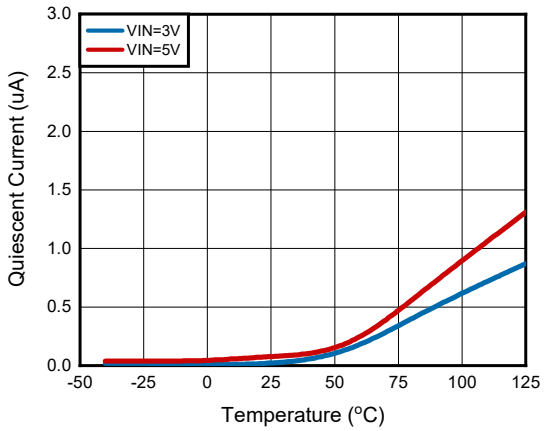


Figure 2. Shutdown Current vs. Temperature

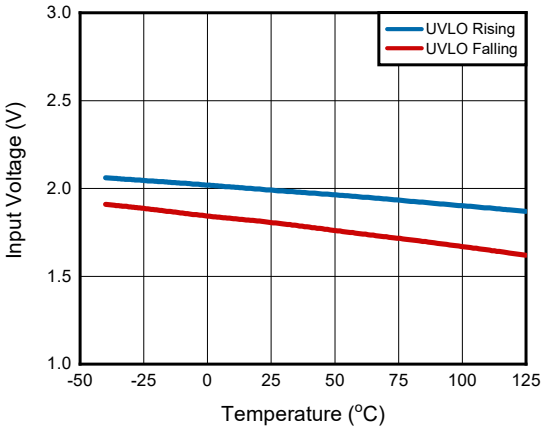


Figure 3. VIN Thresholds vs. Temperature

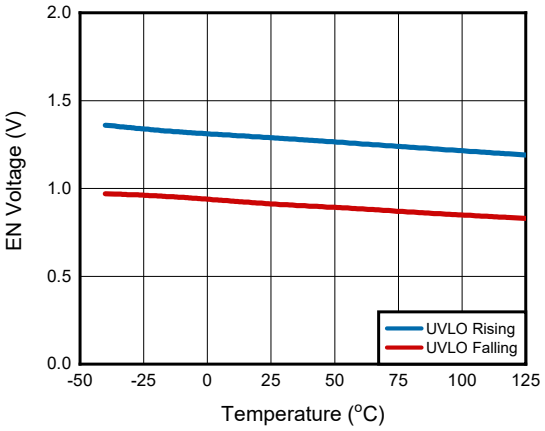


Figure 4. Enable Thresholds vs. Temperature

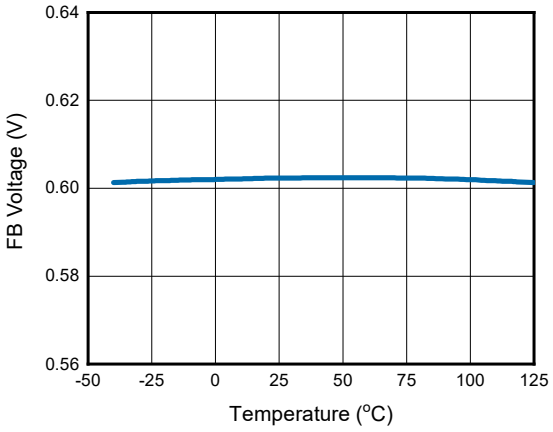


Figure 5. FB Voltage vs. Temperature

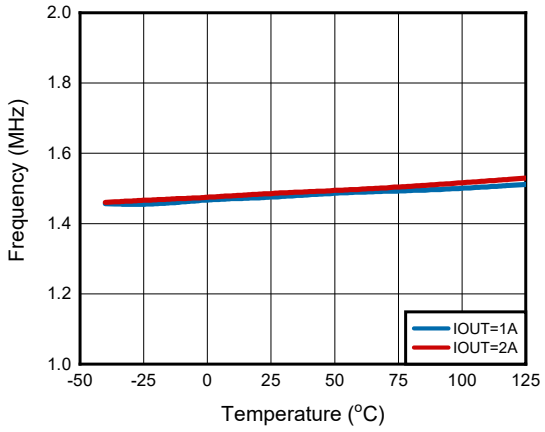


Figure 6. Switch Frequency vs. Temperature

Typical Characteristics (continued)

T_A = -40°C to 125°C, unless otherwise noted.

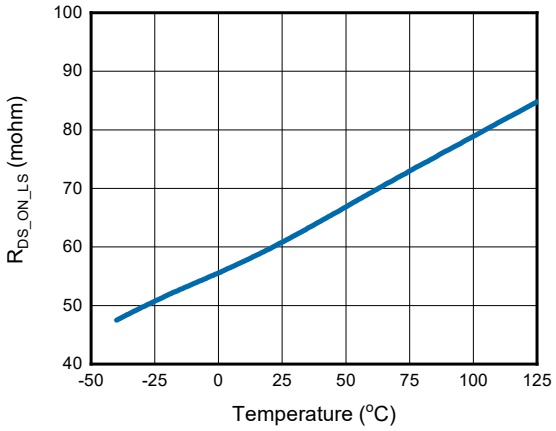


Figure 7. Low-side FET ON Resistance vs. Temperature

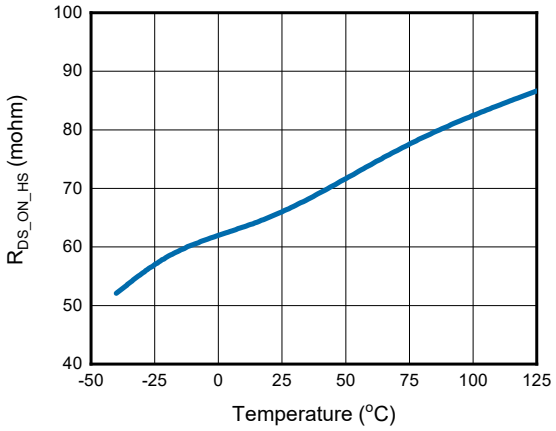


Figure 8. High-side FET ON Resistance vs. Temperature

6 Functional Description

6.1 Block Diagram

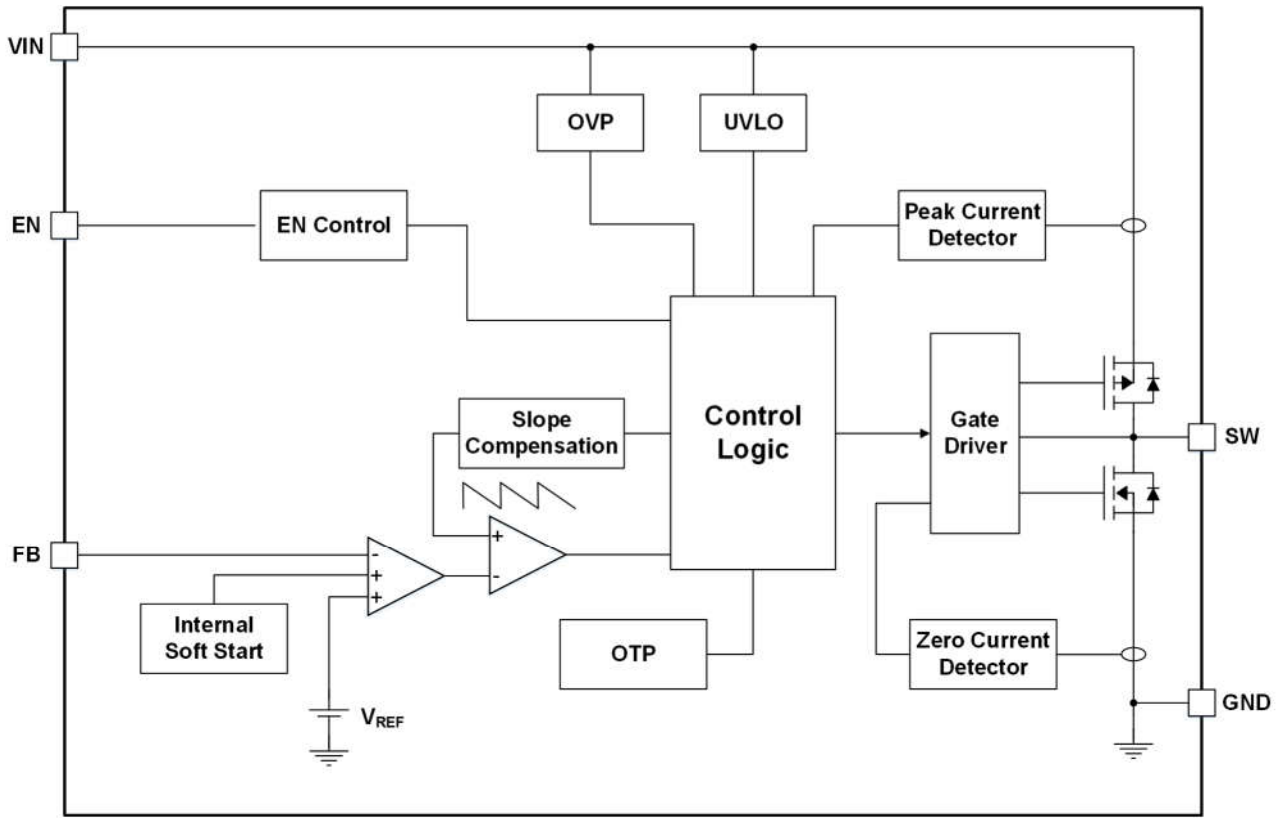


Figure 9. SC1104 Functional Block Diagram

6.2 Operation

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limit for superior load, line response, protection of the internal main switch and synchronous rectifier. The SC1104 switches at a constant frequency and regulates the output voltage. During each cycle, the PWM comparator modulates the power transferred to the load by changing the inductor peak current based on the feedback error voltage. During normal operation, the main switch is turned on for a certain time to ramp the inductor current at each rising edge of the internal oscillator, and switched off when the peak inductor current is above the error voltage. When the main switch is off, the synchronous rectifier will be turned on immediately and stay on until next cycle starts.

6.2.1 Pulse Frequency Modulation

The device automatically enters Pulse Frequency Modulation(PFM) to improve efficiency at light load when the inductor current becomes discontinuous. In discontinuous conduction mode(DCM), the low-side switch is turned off when the inductor current drops to approximately 0A. When feedback voltage(V_{FB}) drops below the reference voltage, the high-side FET is turn on. In PFM mode, the switching frequency is decreased by the control loop to

maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to less frequent switching actions. PFM mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at small loads. This trades off very good light-load efficiency for larger output voltage ripple and variable switching frequency. Also, small increase in output voltage occurs at light loads.

6.2.2 100% Duty Cycle Low Dropout

The device offers a low input-to-output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side FET is switched off.

6.2.3 Soft Startup

The device employs internal soft start function to reduce input inrush current and creates a smooths output voltage rise slope during start up. The internal soft start time is set to 0.7ms.

6.2.4 Input Over Voltage Protection

The device supports input over voltage protection. When input voltage exceeds the input over voltage threshold 6.1V(typical), the regulator will be shutdown unless the input over voltage is removed.

6.2.5 Under Voltage Lockout

To avoid mis-operation of the device at an insufficient supply voltage, implement under voltage locking to shutdown the device when the voltage is below the V_{HYS} hysteresis of the V_{UVLO}.

6.2.6 Short Circuit Protection

The device provides short circuit protection function to prevent the device damaged from short condition. When the short condition occurs and the feedback voltage drops lower than 20% of the regulation level, the oscillator frequency will be reduced and hiccup mode will be triggered to prevent the device from overheating during the extended short condition. Once the short condition is removed, the frequency and current limit will return to normal.

6.2.7 Over Current Protection

The device over current protection function is implemented by using cycle-by-cycle current limit architecture. The inductor current is monitored by measuring the high-side FET series sense resistor voltage. When the load current increases, the inductor current will also increase. When the peak inductor current reaches the current limit threshold 4.0A(typical), the output voltage will start to drop. When the over current condition is removed, the output voltage will return to the regulated value.

6.2.8 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C(typical), both the high-side and low-side FETs are turned off. Once the device temperature falls below the threshold with hysteresis 25°C (typical), the device returns to normal operation automatically.

6.3 Device Mode Description

6.3.1 Device Enable

The device EN pin provides digital control to turn on/off the regulator. When V_{EN} exceeds the threshold voltage, the regulator will start the soft start function. If V_{EN} is below the shutdown threshold voltage, the regulator will turn into the shutdown mode and the shutdown current will be smaller than 1μA. The EN input must be terminated and should not be left floating.

7 Application Information

The SC1104 device is typically used as a step down converter, which convert an input voltage from 2.7V to 5.75V to fixed output voltage 1.2V.

7.1 Typical Application Circuit

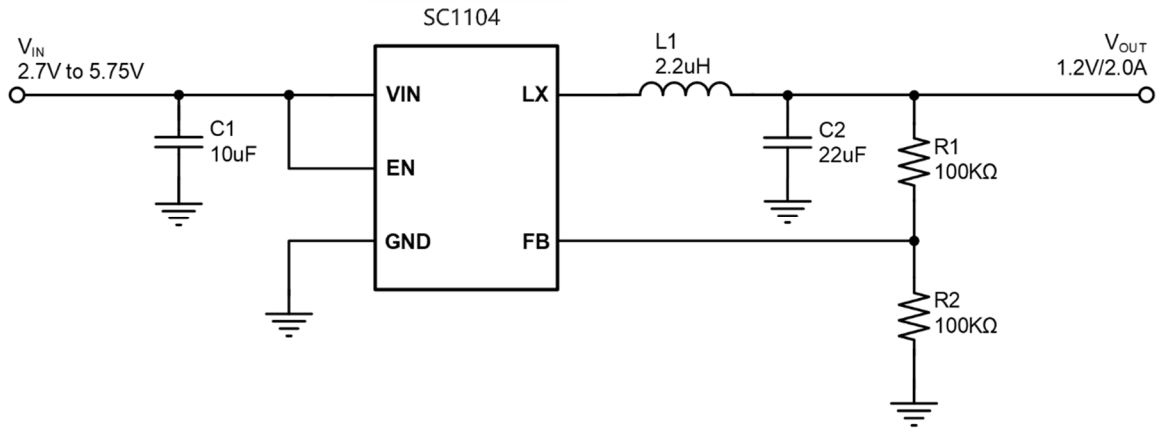


Figure 10. 1.2V, 2A Reference Design

7.2 Design Example

For this design example, use the parameters in Table 1.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input Voltage	2.7V to 5.75V
Output Voltage	1.2V
Maximum Output Current	2A

Table 2 lists the components used for the example.

Table 2. Design Example Component[1,2]

COMPONENT	DESCRIPTION
C1	10uF, Ceramic Capacitor, 10V, X7R, size 0603
C2	22uF, Ceramic Capacitor, 10V, X7R, size 0603
L1	2.2uH, Power Inductor
R1,R2	Divider resistor, 1%, size 0603
C3*	Optional, 10pF if it is needed. Meanwhile, C2 recommends using 10uF

1. The components used in these design cases do not belong to Steadichips products, Steadichps does not warrant its accuracy or completeness. Customers need to test and verify whether the selected components meet their intended use to ensure stable system operation.
2. Refer to *Detailed Design Description* section for guidance on component selection and calculation equations.

7.3 Detailed Design Description

7.3.1 Output Voltage Setting

An external resistor divider is used to set output voltage according to Equation(1). By selecting R1 and R2, the output voltage is programmed to the desired value. When the output voltage is regulated, the typical voltage reference at the FB pin is 0.6V.

To ensure system performance, choose the value of R2 carefully. Since a large R2 make FB sensitive to noise and a small R2 increase power loss. So the value of 100KΩ is recommended. It can achieves a balance between system stability and low current consumption.

$$V_{OUT} = 0.6V \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

The feedback circuit is shown in Figure 11.

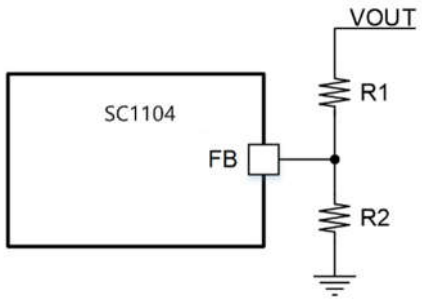


Figure 11. Feedback resistor divider

Table 3 lists the recommended parameters values for common output voltages.

Table 3. Component selection for common output voltages

V_{OUT}(V)	R1(KΩ)	R2(KΩ)	L(uH)
3.3	453	100	2.2uH
2.5	316	100	2.2uH
1.8	200	100	2.2uH
1.5	150	100	2.2uH
1.2	100	100	2.2uH
1.05	75	100	2.2uH

7.3.2 Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (ISAT), and DC resistance (DCR). In general, inductors with larger inductance and low DCR values provide much more output and high conversion efficiency, and smaller inductance values can give batter load transient response.

A good compromise between size and loss is to choose the peak-to-peak ripple current equals to 20% to 40% of the IC rated current. And the peak inductor current can be calculated by Equation(2) and Equation(3). Ensure that

the peak inductor current is below the maximum switch current.

$$\Delta I_L = (0.2 \text{ to } 0.4) \times I_{OUT(MAX)} \tag{2}$$

$$I_{L(peak)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2} \tag{3}$$

The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value according to Equation(4). Once an inductor value is chosen, the peak inductor current is determined by Equation(3). Attention that the inductor should not saturate under the inductor peak current.

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_{SW} \times \Delta I_L} \tag{4}$$

7.3.3 Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to do this without causing a large variation in input voltage. The input capacitance value determines the input voltage ripple of the converter. For most applications, a 10μF capacitor is sufficient.

The peak-to-peak voltage ripple on input capacitor can be estimated with Equation(5):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{5}$$

For best performance, ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. To compensate the derating of the ceramic capacitors, the voltage rating of capacitor should be twice of the maximum input voltage. The input capacitor also requires an adequate ripple current rating since it absorbs the input switching current.

The input ripple current can be estimated with Equation(6):

$$I_{CIN} = I_{OUT} \times \sqrt{D \times (1 - D)} \tag{6}$$

Where D is the duty cycle of converter. The worst-case condition occurs at $V_{IN} = 2V_{OUT}$. At this point, the input ripple current of input capacitance is equal to half of output current. For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

7.3.4 Output Capacitor Selection

The output capacitor stabilizes the DC output voltage, it directly affects the steady state, output voltage ripple, loop stability, and output voltage overshoot and undershoot during load current transient.

The output voltage ripple can be estimated with Equation(7):

$$\Delta V_{OUT} = \Delta I_L \times \left(C_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right) \tag{7}$$

The output capacitor ripple is essentially composed of two part. One part is caused by the inductor ripple current flowing through the ESR of output capacitors, another part is caused by the inductor ripple current charging and

discharging output capacitors. For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. And when using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple.

The output capacitance must be large enough to supply the current when a large load step occurs. But if the output capacitor value is too high, the output voltage will not be able to reach the design value during the soft start time. A 10uF Ceramic capacitors are recommended in this application.

7.4 Power Dissipation

For DC/DC, these is still some power deposited on the chip and converted into heat, in spite of switch mode power supplies have considerably higher efficiency when compared to linear regulators. The device power dissipation includes conduction loss, switching loss, gate charge loss and quiescent current losses. The maximum allowable continuous power dissipation at any ambient temperature is calculated by Equation(8):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (8)$$

Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction to ambient thermal resistance. Once exceeding the maximum allowable power, The device enters thermal shutdown to avoid permanent damage.

7.5 Typical Application Curves

T_A = 25°C, unless otherwise noted.

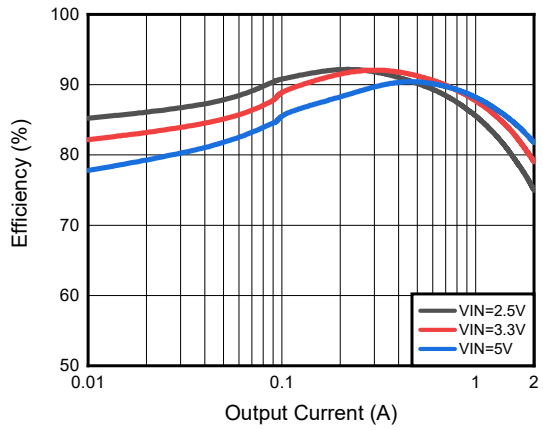


Figure 12. 1.2V Output Efficiency

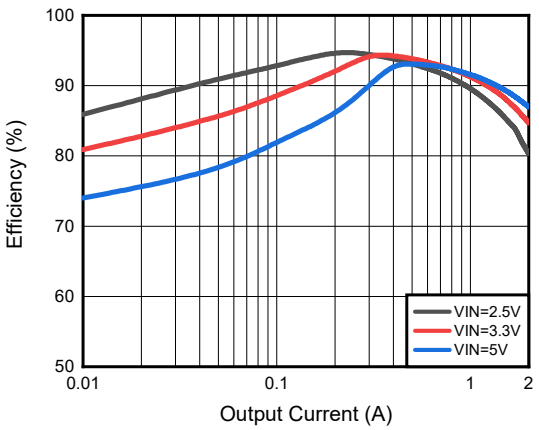


Figure 13. 1.8V Output Efficiency

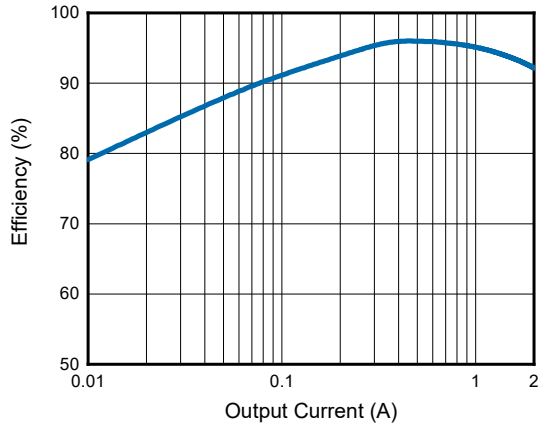


Figure 14. 3.3V Output Efficiency

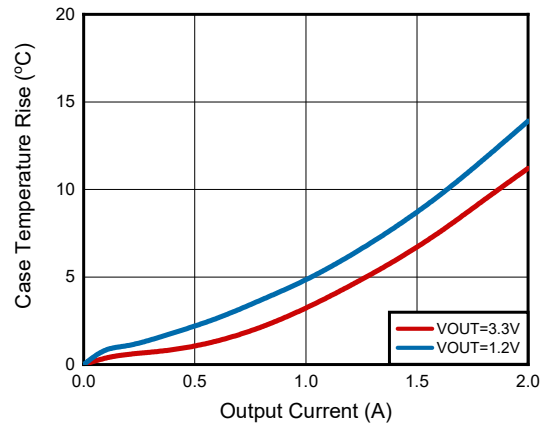


Figure 15. Case Temperature

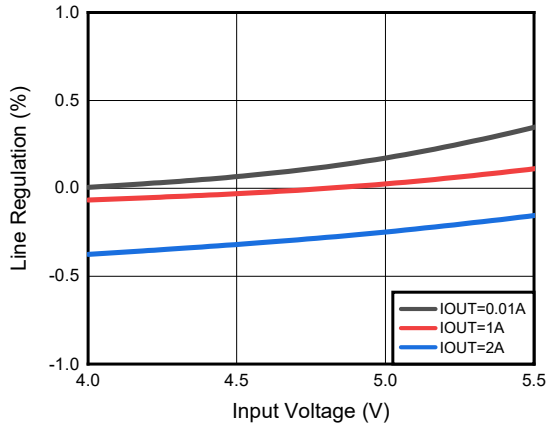


Figure 16. Line Regulation (V_{OUT} = 3.3V)

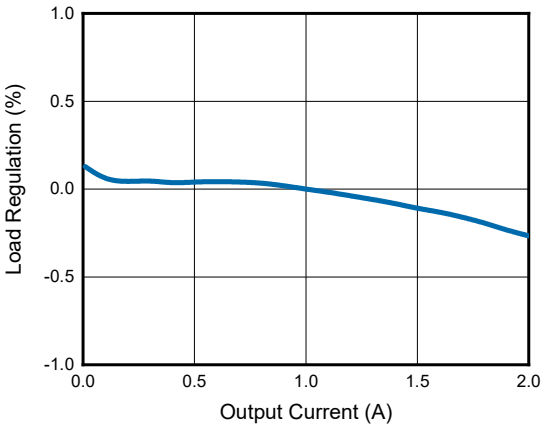
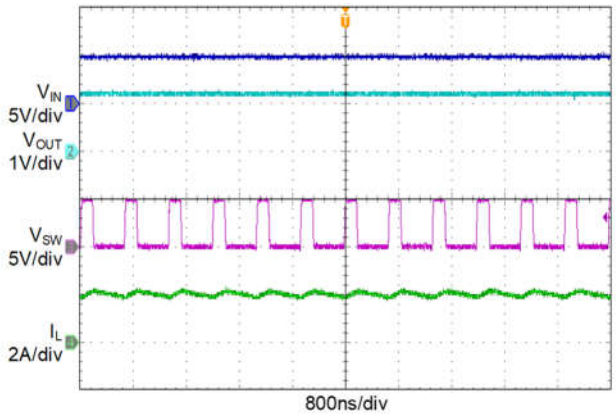


Figure 17. Load Regulation (V_{OUT} = 3.3V)

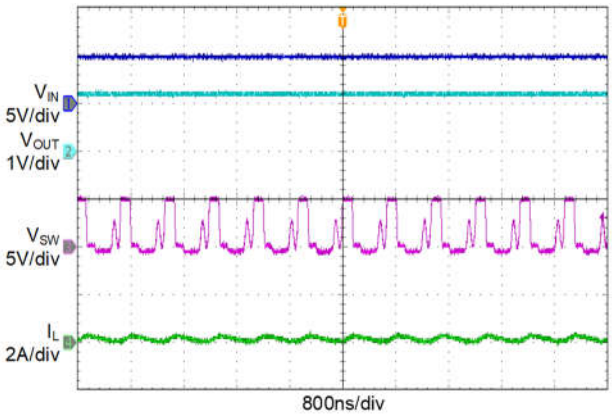
Typical Application Curves (continued)

V_{IN} = 5V, V_{OUT} = 1.2V, L = 2.2uH, T_A = 25°C, unless otherwise noted.



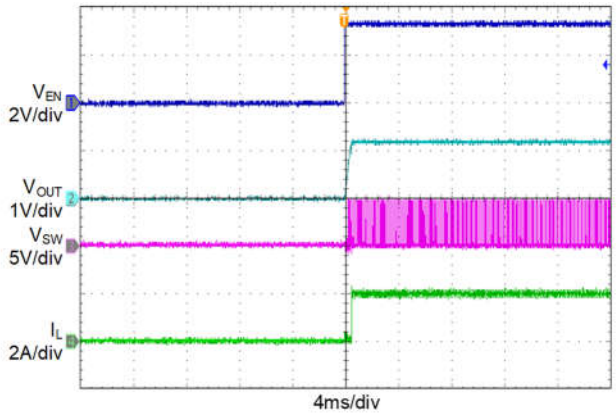
I_{OUT} = 2.0A

Figure 18. PWM Operation



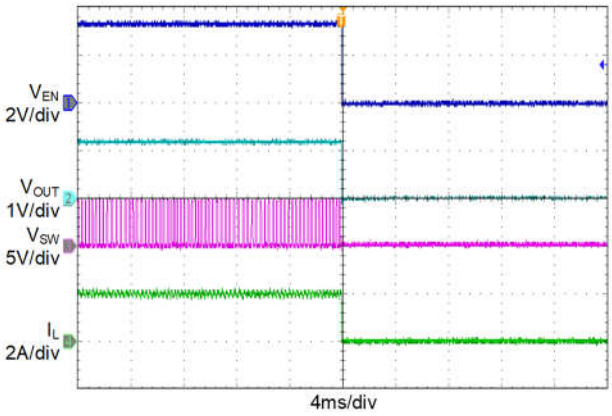
I_{OUT} = 0.1A

Figure 19. Save Mode Operation



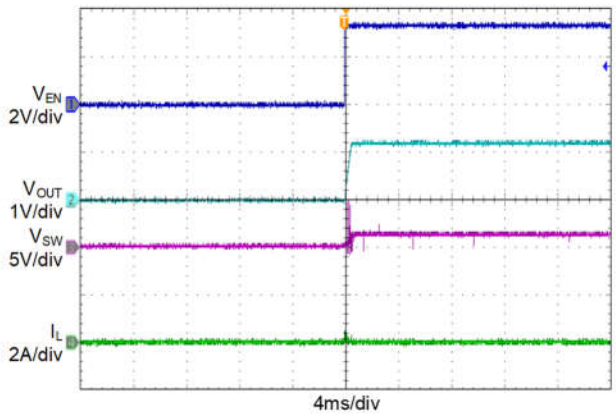
I_{OUT} = 2.0A

Figure 20. EN StartUp with Load

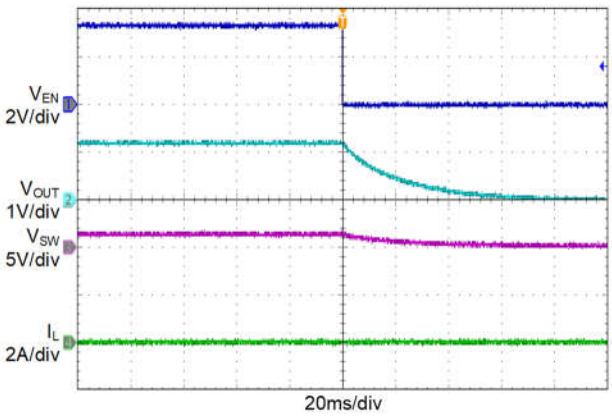


I_{OUT} = 2.0A

Figure 21. EN ShutDown with Load



I_{OUT} = 0A

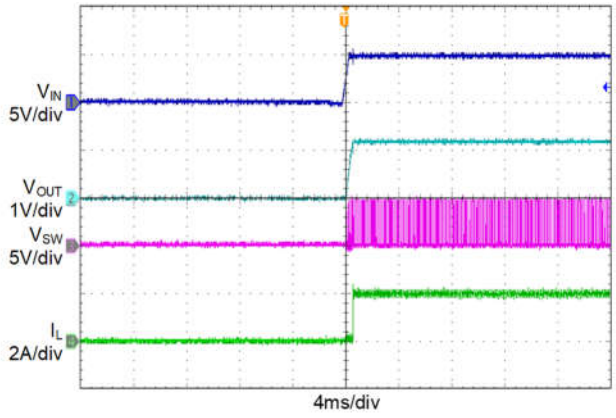


I_{OUT} = 0A

Figure 22. EN StartUp without Load	Figure 23. EN ShutDown without Load

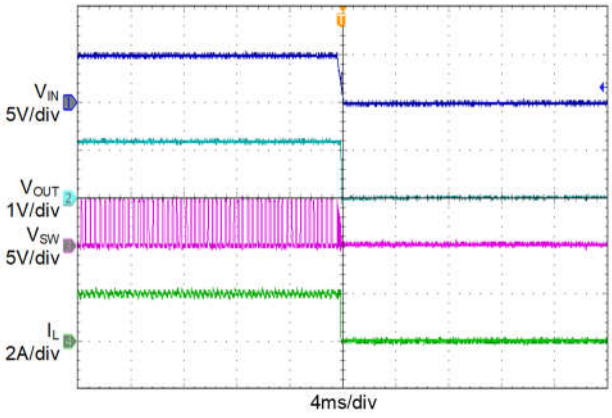
Typical Application Curves (continued)

V_{IN} = 5V, V_{OUT} = 1.2V, L = 2.2uH, T_A = 25°C, unless otherwise noted.



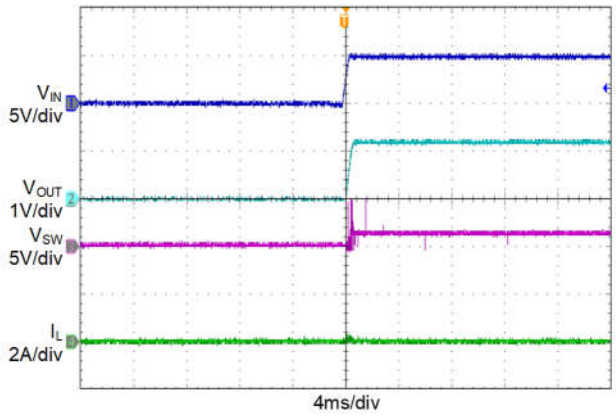
I_{OUT} = 2.0A

Figure 24. VIN StartUp with Load



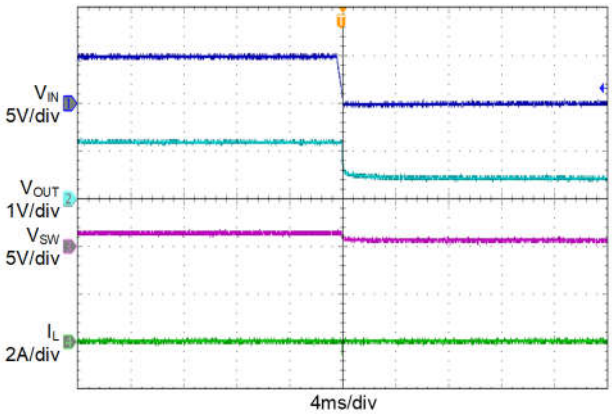
I_{OUT} = 2.0A

Figure 25. VIN ShutDown with Load



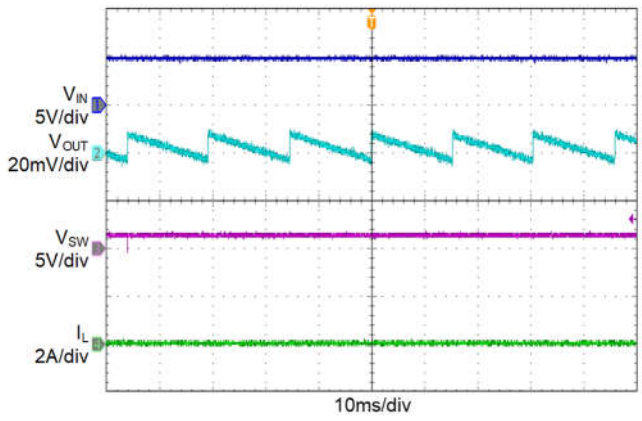
I_{OUT} = 0A

Figure 26. VIN StartUp without Load



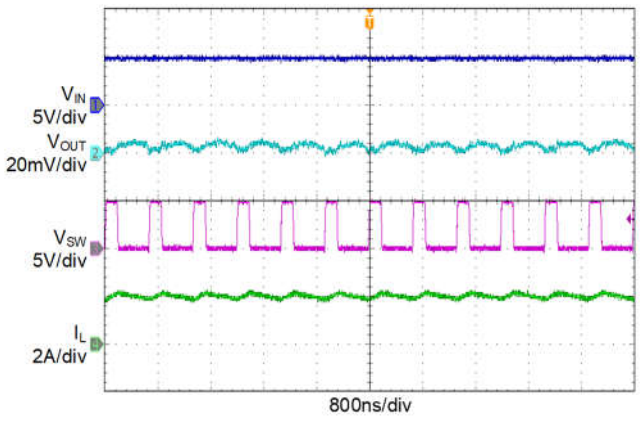
I_{OUT} = 0A

Figure 27. VIN ShutDown without Load



I_{OUT} = 0A

Figure 28. Output Ripple without Load

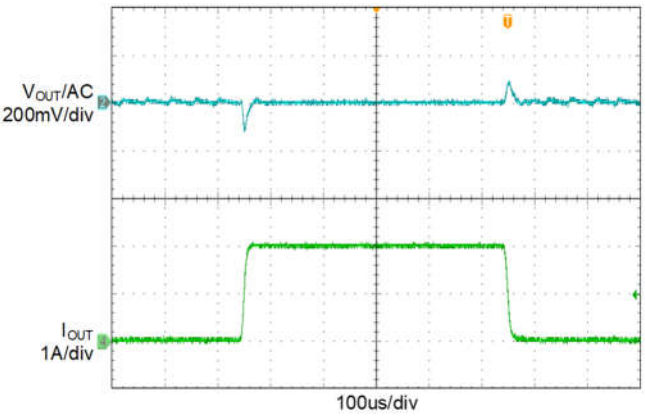


I_{OUT} = 2.0A

Figure 29. Output Ripple with Load

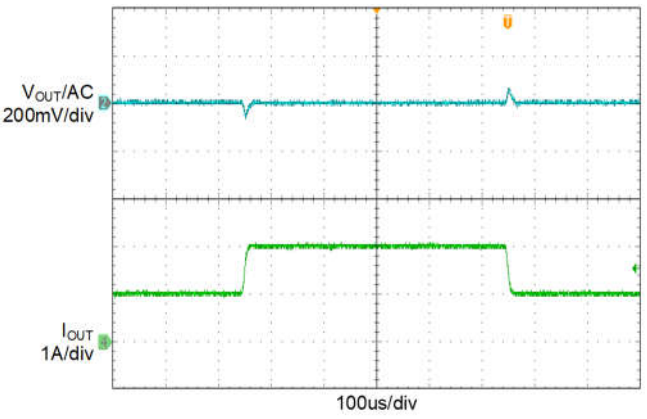
Typical Application Curves (continued)

VIN = 5V, VOUT = 1.2V, L = 2.2uH, T_A = 25°C, unless otherwise noted.



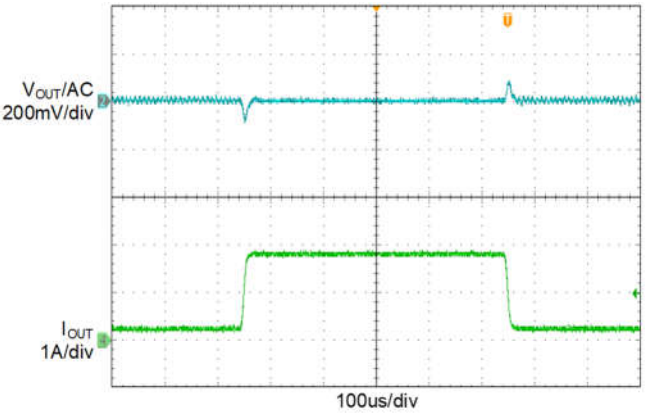
I_{OUT} = 0A to 2.0A, 1A/us slew rate

Figure 30. Transient Response



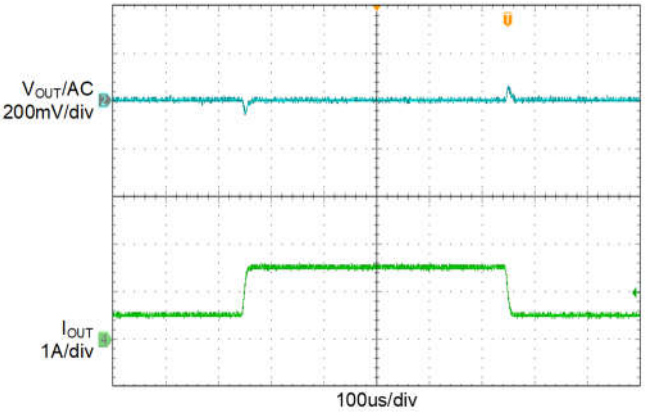
I_{OUT} = 1.0A to 2.0A, 1A/us slew rate

Figure 31. Transient Response



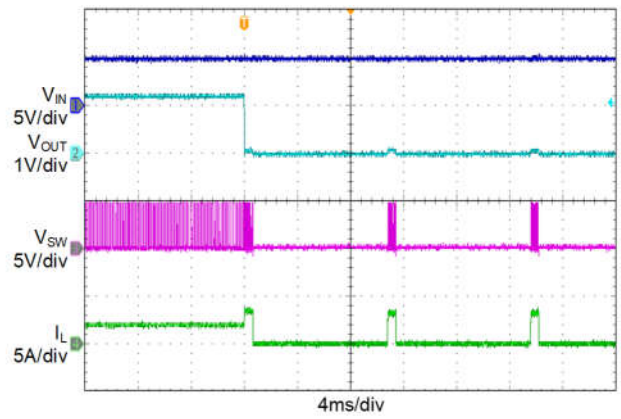
I_{OUT} = 0.2A to 1.8A, 1A/us slew rate

Figure 32. Transient Response



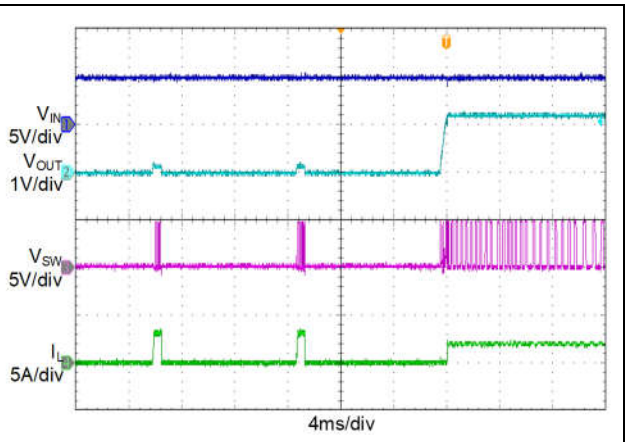
I_{OUT} = 0.5A to 1.5A, 1A/us slew rate

Figure 33. Transient Response



I_{OUT} = 2.0A

Figure 34. SCP Entry



I_{OUT} = 2.0A

Figure 35. SCP Recovery

8 Layout Guidelines and Example

Efficient PCB layout is critical for stable operation. For the high-frequency switching converter, a poor layout design can result in poor line or load regulation and stability issues.

1) Place the input/output capacitor and inductor should be placed as close to IC.
2) Keep the power traces as short as possible.
3) The low side of the input and output capacitor must be connected properly to the power GND avoid a GND potential shift.
4) Place the external feedback resistors next to FB.
5) Keep the switching node SW short and away from the feedback network.

For best results, follow the layout example below.

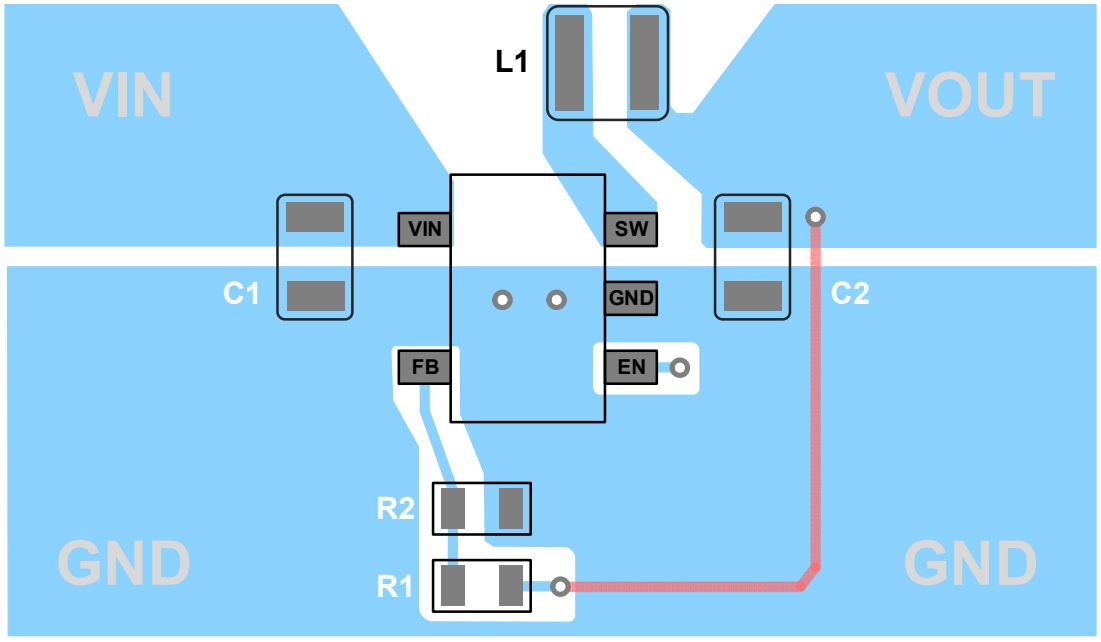
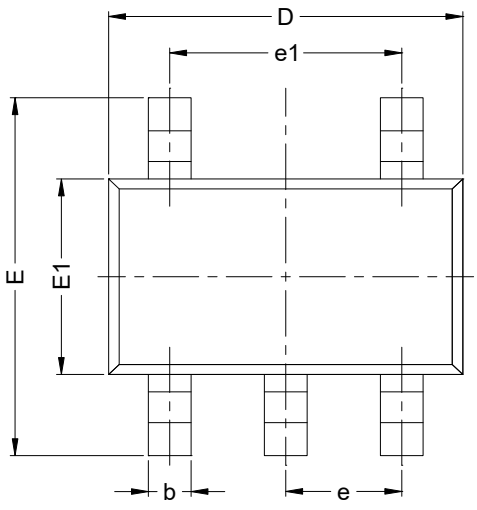


Figure 36. Typical SC1104 Example Layout

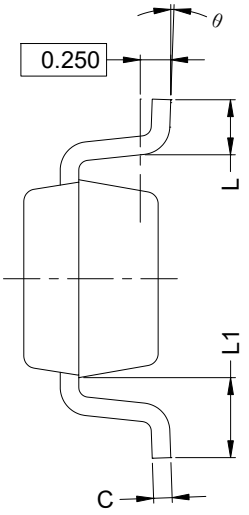
9 Package Information

9.1 Outline Dimensions

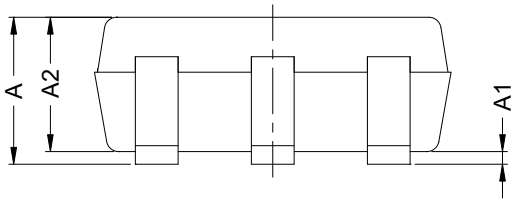
SOT23-5 Package Outline



TOP VIEW



SIDE VIEW



FRONT VIEW

NOTES:

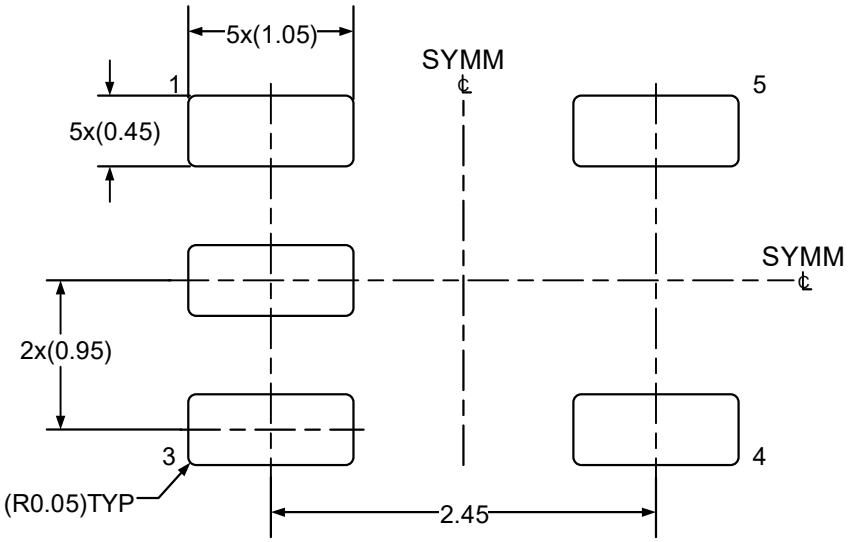
1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 4 *SOT23-5 dimensions(mm)*.

Table 4. SOT23-5 dimensions(mm)

SYMBOL	MIN	TYP	MAX
A			1.25
A1	0.03	0.08	0.15
A2	1.05	1.10	1.15
b	0.27		0.35
c	0.135		0.23
D	2.82	2.92	3.02
E	2.60	2.90	3.00
E1	1.50	1.62	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.35	0.45	0.55
L1	0.49	0.64	0.79
θ	0°		8°

9.2 Recommended Land Pattern

SOT23-5 Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Explosed metal shown.
3. Drawing is 20X scale.

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
SC1104NSTR-I	SOT23-5	Green	Tape & Reel	3000	Industrial -40°C to +85°C