SC8833
Dual H-Bridge Motor Driver

1 Features

- Dual-H-Bridge Current-Control Motor Driver
  - 1 or 2 DC Motors or 1 Stepper Motor
  - Low-MOSFET ON-Resistance: HS + LS 1.0Ω (Typical,25℃)
- Output Current Capability(at Vm=5V,25℃)
  - eTSSOP Package
    - 1.0 A RMS, 1.2 A Peak per H-Bridge
    - 2.0 A RMS in Parallel Mode
  - QFN Package
    - 0.9 A RMS, 1.2 A Peak per H-Bridge
    - 1.8 A RMS in Parallel Mode
- Wide Power Supply Voltage
  - 2.5 V to 10.8 V
- Integrated Current Regulation
- Easy Pulse-Width-Modulation (PWM) Interface
- 120-nA Low-Power Sleep Mode (at 5 V)
- Small Package and Footprint
  - 16 eTSSOP (With Thermal Pad) 5.00 x 6.40 mm
  - 16 QFN (With Thermal Pad) 3.00 x 3.00 mm
- Protection Features
  - VM Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - Fault Indication Pin(nFAULT)

2 Applications

- Point-of-Sale Printers
- Video Security Cameras
- Office Automation Machines
- Gaming Machines
- Robotics
- Battery-Powered Toys

3 Description

The SC8833 provides a dual-bridge motor driver solution for cameras, printers, toys, robotics and other mechatronic applications.

The device has two H-bridge drivers, and drive two DC brushed motors, a bipolar stepper motor, solenoids, or other inductive loads.

The output driver block consists of N-channel power MOSFETs configured as an H-bridge to drive the motor winding. An internal charge pump generates gate drive voltages.

With proper PCB design, each H-bridge of The SC8833 can drive up to 1.0 A RMS (or DC) continuously, at 25℃ with a VM supply of 5V. The device can support peak currents of up to 1.2 A per bridge of output current. Current capability is reduced slightly at low VM voltage.

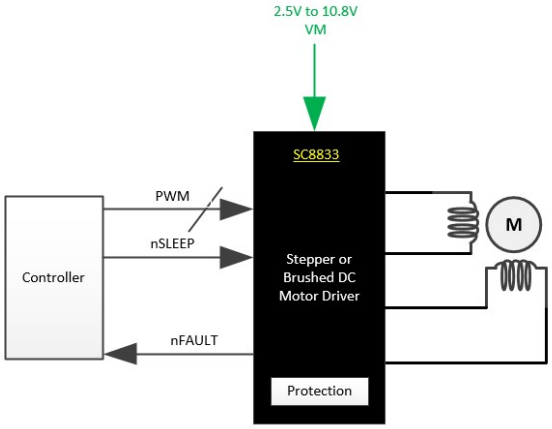
The SC8833 device has two PWM(IN/IN) input interface. Internal shutdown functions with a fault output pin are provided for overcurrent protection, short circuit protection, undervoltage lockout, and overtemperature.

The SC8833 is packaged in a 16-pin eTSSOP and 16-pin QFN package.

Device Information(1)

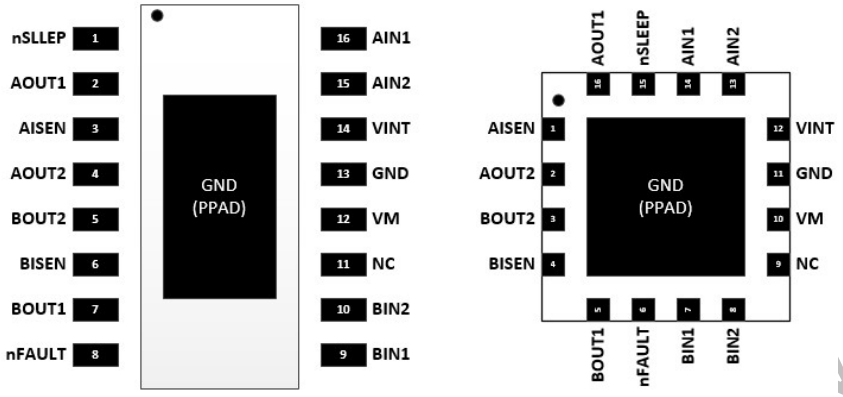
PART NUMBER	PACKAGE	BODY SIZE (NOM)
SC8833S	eTSSOP (16)	5.00 mm × 6.40 mm
SC8833Q	QFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

4 Pin Configuration and Functions



Pin Functions

PIN			TYPE	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	eTSSOP	QFN			
POWER AND GROUND					
GND, Thermal pad	13	11	PWR	Device ground	This pin must be connected to the PCB ground
VINT	14	12	—	Internal regulator	Bypass to GND with a 2.2uF,6.3V capacitor
VM	12	10	PWR	Device power supply	Connect to motor supply. A 10uF(minimum) ceramic bypass capacitor to GND is recommended
CONTROL					
AIN1	16	14	I	Bridge A input 1	Controls the state of AOUT1 and AOUT2
AIN2	15	13	I	Bridge A input 2	Internal pulldown
BIN1	9	7	I	Bridge B input 1	Controls the state of BOUT1 and BOUT2
BIN2	10	8	I	Bridge B input 2	Internal pulldown
nSLEEP	1	15	I	Sleep mode input	Logic high to enable device; Logic low to enter low-power sleep mode and reset all internal logic; Internal pulldown
STATUS					
nFAULT	8	6	OD	Fault output	Logic low when in fault condition (overtemperature, overcurrent)
OUTPUT					
AISEN	3	1	IO	Bridge A ground/Isense	Connect to current sense resistor for bridge A or GND if current control not needed
BISEN	6	4	IO	Bridge B ground/Isense	Connect to current sense resistor for bridge B or GND if current control not needed
AOUT1	2	16	O	Bridge A output 1	Connect to motor winding A
AOUT2	4	2	O	Bridge A output 2	
BOUT1	7	5	O	Bridge B output 1	Connect to motor winding B
BOUT2	5	3	O	Bridge B output 2	

5 Specifications

5.1 Absolute Maximum Ratings

See(1)(2)

		MIN	MAX	UNIT
	Power supply voltage, VM	-0.3	12	V
	Internal regulator, VINT	-0.3	3.8	V
	Digital input pin voltage	-0.5	7.0	V
	Peak motor drive output current	Internally limited		A
T_J	Operating junction temperature	-40	150	℃
T_{stg}	Storage temperature	-60	150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS－001(1)	±3000	V
	Charge-device model (CDM), per JEDEC specification JESD22－C101(1)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5. 3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage(1)		2.5		10.8	V
V_{IN}	Logic level input voltage		0		5.5	V
I_{RMS}	Motor RMS current(2)	HTSSOP16 Package	0		1.0	A
		QFN16 Package	0		0.9	A
f_{pwm}	Externally applied PWM frequency		0		200	kHz
T_A	Operating ambient temperature		-40		85	℃

(1) Note that when V M is below 5 V, R DS(ON) increases and maximum output current is reduced.

(2) Power dissipation and thermal limits must be observed.

5.4 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (V_M, VINT)						
V_M	VM operating voltage		2.5		10.8	V
I_{VM}	VM operating supply current	V_M = 5 V, xINx low, nSLEEP high		0.6	1.0	mA
I_{VMQ}	VM sleep mode supply current	V_M = 5 V, nSLEEP low		30	95	nA
t_{SLEEP}	Sleep time	nSLEEP low to sleep mode		10		µs
t_{WAKE}	Wake-up time	nSLEEP high to output transition		155		µs
t_{ON}	Turn-on time	V_M > V_{UVLO} to output transition		25		µs
VINT	Internal regulator voltage	V_M = 5 V	3.2	3.5	3.8	V
V_{UVLO}	VM undervoltage lockout voltage	V_M rising			2.5	V
		V_M falling			2.4	V
LOGIC-LEVEL INPUTS (AIN1, AIN2, BIN1, BIN2, nSLEEP)						
V_{IL}	Input low voltage	xINx	0		0.7	V
		nSLEEP	0		0.5	V
V_{IH}	Input high voltage	xINx	1.8		5.5	V
		nSLEEP	2.3		5.5	V
V_{HYS}	Input logic hysteresis		200	300	500	mV
I_{IL}	Input low current	V_{IN}=0	-5		5	µA
I_{IH}	Input high current	V_{IN}=5.0V			50	µA
P_{PD}	Pulldown resistance			100		KΩ
t_{DEG}	Input deglitch time				600	ns
t_{PROP}	Propagation delay INx to OUTx	V_M = 5 V			1.2	µs
CONTROL OUTPUT (nFAULT)						
V_{OL}	Output logic low voltage	I_O=5 mA			0.1	V
I_{OH}	Output logic high leakage	R_{PULLUP}=1KΩ to 5 V	-1		1	µA
MOTOR DRIVER OUTPUTS(AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ON)}$	High-side FET on resistance	V_M=5V,I_O=0.2A,T_j=−40℃ (1)		400		mΩ
		V_M=5V,I_O=0.2A,T_j=25℃		550		mΩ
		V_M=5V,I_O=0.2A,T_j=85℃ (1)		650		mΩ
		V_M=2.7V,I_O=0.2A,T_j=−40℃ (1)		650		mΩ
		V_M=2.7V,I_O=0.2A,T_j=25℃		800		mΩ
		V_M=2.7V,I_O=0.2A,T_j=85℃ (1)		900		mΩ
$R_{DS(ON)}$	Low-side FET on resistance	V_M=5V,I_O=0.2A,T_j=−40℃ (1)		350		mΩ
		V_M=5V,I_O=0.2A,T_j=25℃		450		mΩ
		V_M=5V,I_O=0.2A,T_j=85℃ (1)		550		mΩ
		V_M=2.7V,I_O=0.2A,T_j=−40℃ (1)		650		mΩ
		V_M=2.7V,I_O=0.2A,T_j=25℃		800		mΩ
		V_M=2.7V,I_O=0.2A,T_j=85℃ (1)		900		mΩ

I_{OFF}	OFF-state leakage current	V_M=5V	-1		1	μA
t_{RISE}	Output rise time	V_M = 5 V; R_L = 16Ω to GND		70		ns
t_{FALL}	Output fall time	V_M = 5 V; R_L = 16Ω to V_M		80		ns
t_{DEAD}	Dead time(2)	V_M = 5 V		450		ns
PWM CURRENT CONTROL (AISEN, BISEN)						
V_{TRIP}	xISEN trip voltage		160	200	240	mV
t_{OFF}	Current control constant off time	Internal PWM constant off time		23		μs
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		1.2			A
t_{DEG}	Overcurrent de-glitch time			1		μs
t_{OCR}	Overcurrent protection retry time			1.4		ms
T_{TSD} (1)	Thermal shutdown temperature	Die temperature, T_J	150			℃
T_{HYS}	Thermal shutdown hysteresis	Die temperature, T_J		20		℃

(1) Not tested in production; based on design and characterization data

6 Detailed Description

6.1 Overview

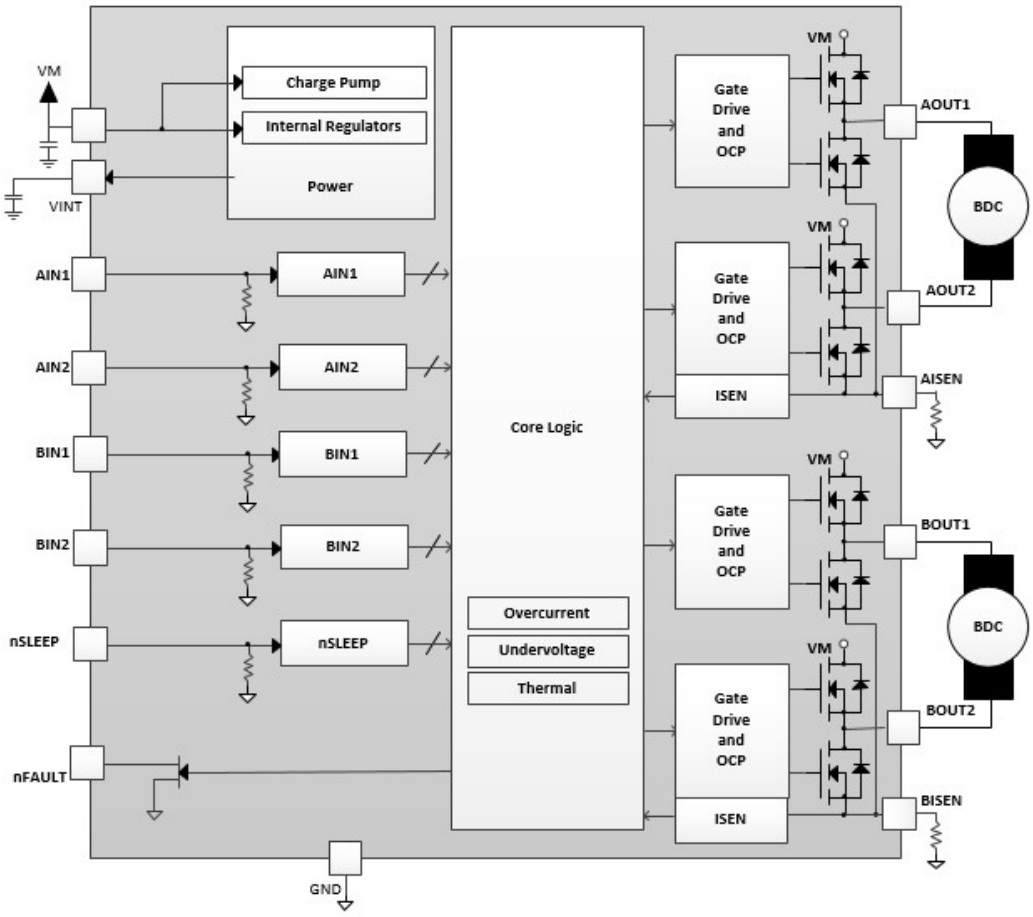
The SC8833 device is an integrated motor driver solution for brushed DC or bipolar stepper motors. The device integrates two NMOS + NMOS H-bridges and current regulation circuitry. The SC8833 can be powered with a supply voltage from 2.5 to 10.8 V and can provide an output current up to 1.0 A RMS.

A simple PWM interface allows easy interfacing to the controller circuit.

The current regulation is a 23-µs fixed off-time slow decay.

The device includes a low-power sleep mode, which lets the system save power when not driving the motor.

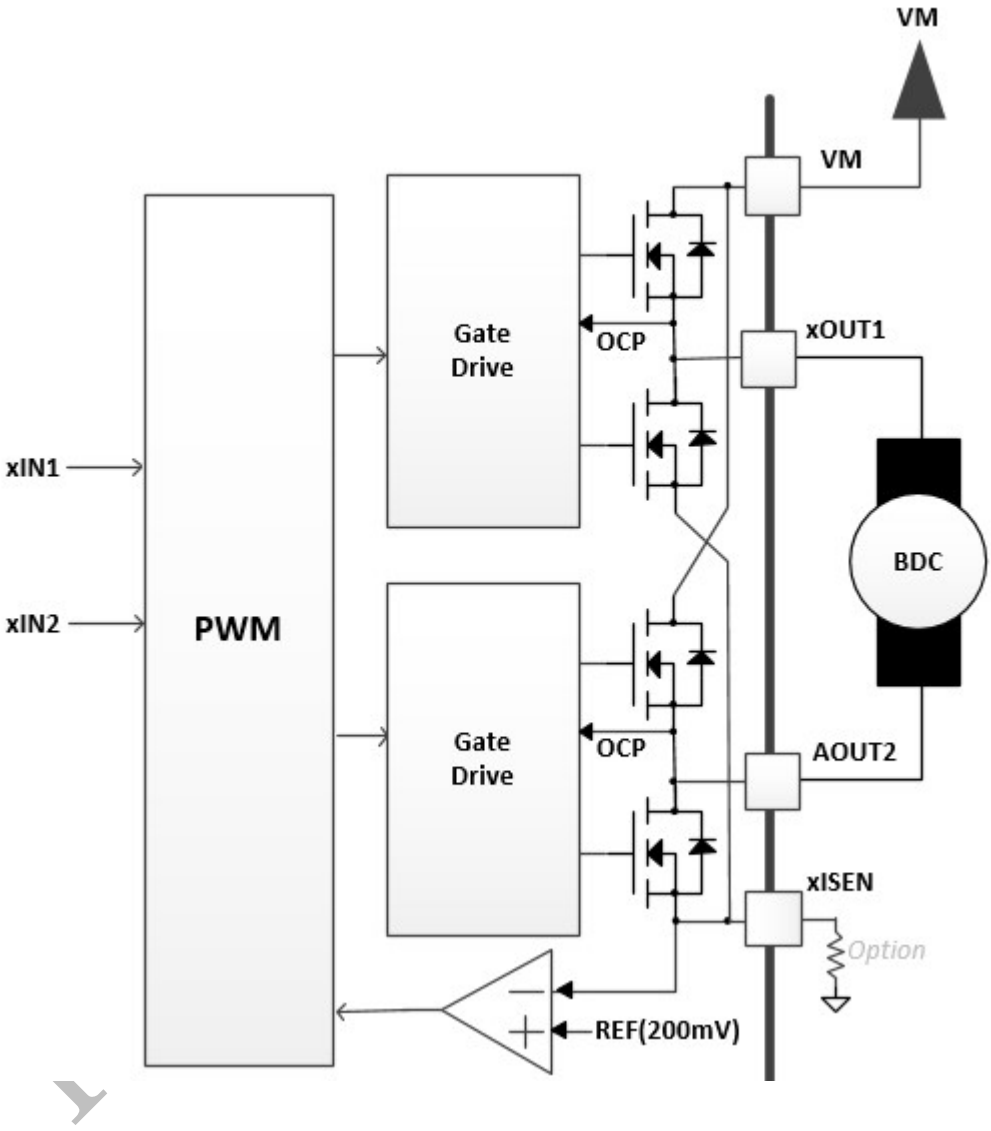
6.2 Functional Black Diagram



6.3 Feature Description

6.3.1 PWM Motor Drivers

The SC8833 contains drivers for two full H-bridges. Figure shows a block diagram of the circuitry.



6.3.2 Bridge Control and Decay Modes

The AIN1 and AIN2 input pins control the state of the AOUT1 and AOUT2 outputs; similarly, the BIN1 and BIN2 input pins control the state of the BOUT1 and BOUT2 outputs (see Table 1).

Table 1. H-Bridge Logic

xIN1	xIN2	xOUT1	xOUT2	FUNCTION
0	0	Z	Z	Coast/ fast decay
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake/ slow decay

The inputs can also be used for PWM control of the motor speed. When controlling a winding with PWM and the drive current is interrupted, the inductive nature of the motor requires that the current must continue to flow (called recirculation current). To handle this recirculation current, the H-bridge can operate in two different states, fast decay or slow decay. In fast-decay mode, the H-bridge is disabled and recirculation current flows through the body diodes. In slow-decay mode, the motor winding is shorted by enabling both low-side FETs.

To externally pulse-width modulate the bridge in fast-decay mode, the PWM signal is applied to one xIN pin while the other is held low; to use slow-decay mode, one xIN pin is held high. See Table 2 for more information.

Table 2. PWM Control of Motor Speedc

xIN1	xIN2	FUNCTION
PWM	0	Forward PWM, fast decay
1	PWM	Forward PWM, slow decay
0	PWM	Reverse PWM, fast decay
PWM	1	Reverse PWM, slow decay

The internal current control is still enabled when applying external PWM to xIN. To disable the current control when applying external PWM, the xISEN pins should be connected directly to ground.

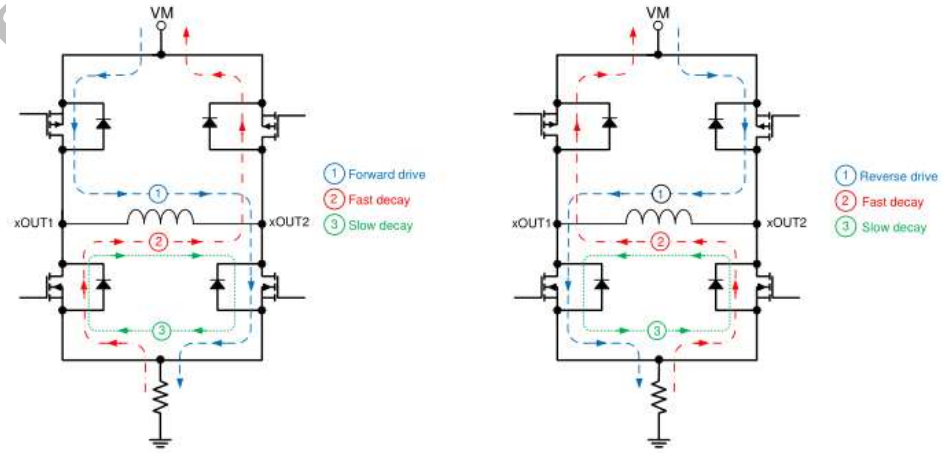


Figure shows the current paths in different drive and decay modes.

6.3.3 Current Control

The current through the motor windings may be limited, or controlled, by a 23-µs constant off-time PWM current regulation, or current chopping. For DC motors, current control is used to limit the start-up and stall current of the motor. For stepper motors, current control is often used at all times.

When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. If the current reaches the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle. Note that immediately after the output is enabled, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 µs.

The PWM chopping current is set by a comparator that compares the voltage across a current sense resistor connected to the xISEN pins with a reference voltage. The reference voltage, V_{TRIP} , is fixed at 200 mV nominally.

The chopping current is calculated as in Equation 1.

$$\mathbf{I_{CHOP}} = \frac{\mathbf{200mV}}{\mathbf{R_{xISEN}}} \quad (1)$$

Example: If a 1-Ω sense resistor is used, the chopping current will be 200 mV / 1 Ω = 200 mA.

NOTE

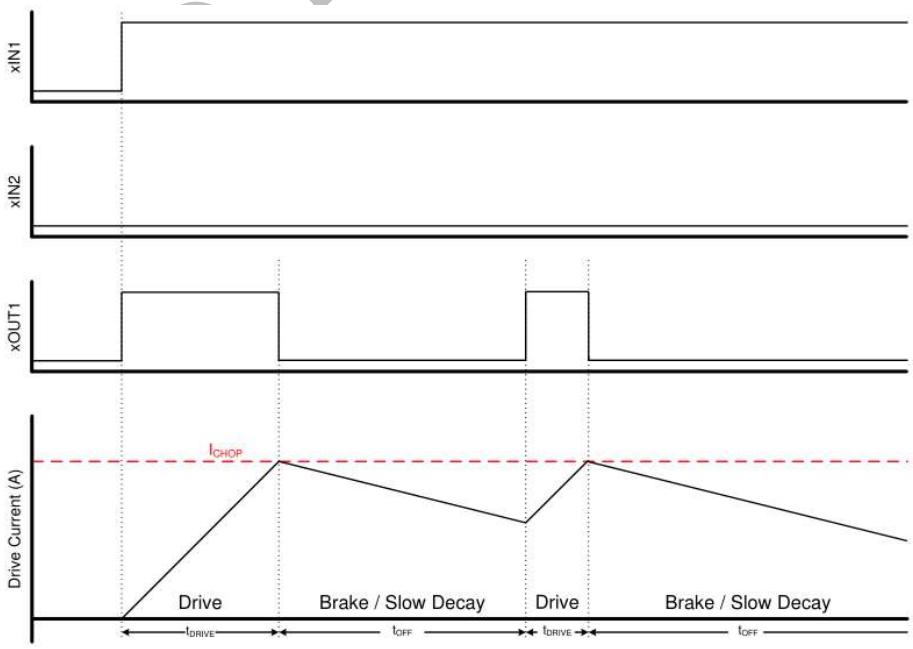
If current control is not needed, the xISEN pins should be connected directly to ground.

6.3.4 Decay Mode

After the chopping current threshold is reached, the H-bridge switches to slow-decay mode. This state is held for t_{off} (23 µs) until the next cycle to turn on the high-side MOSFETs.

6.3.5 Slow Decay

In slow-decay mode, the high-side MOSFETs are turned off and both of the low-side MOSFETs are turned on. The motor current decreases while flowing in the two low-side MOSFETs until reaching its fixed off time (typically 23 µs). After that, the high-side MOSFETs are enabled to increase the winding current again.

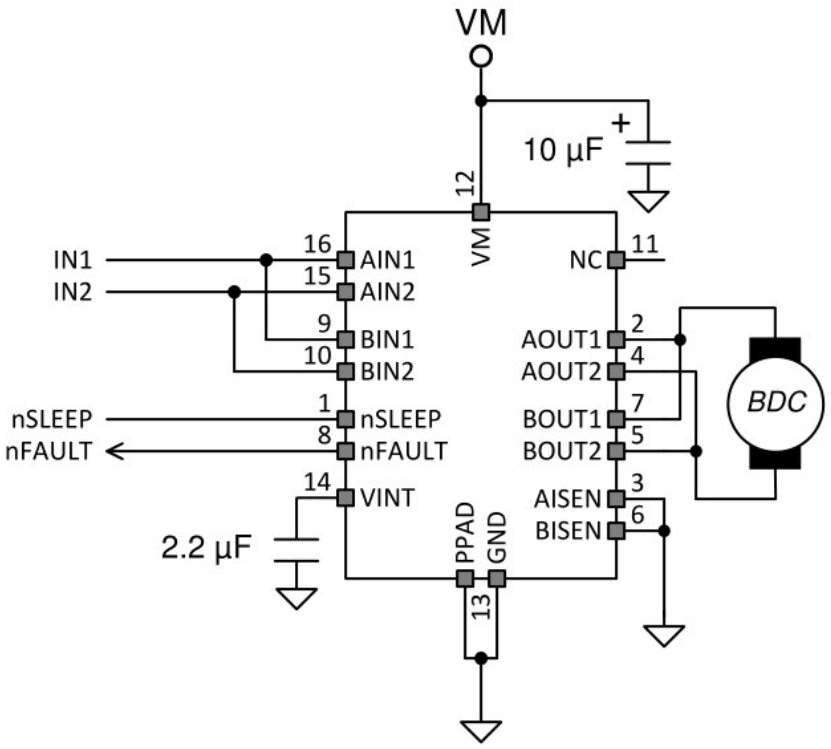


6.3.6 Sleep Mode

Driving nSLEEP low puts the device into a low-power sleep state. In this state, the H-bridges are disabled, all internal logic is reset, and all internal clocks are stopped. All inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time, t_{WAKE} , needs to pass before the motor driver becomes fully operational.

6.3.7 Parallel Mode

The two H-bridges in the SC8833 can be connected in parallel for double the current of a single H-bridge. The internal dead time in the SC8833 prevents any risk of cross-conduction (shoot-through) between the two bridges due to timing differences between the two bridges. Figure shows the connections as follow.



6.3.8 Protection Circuits

The SC8833 is fully protected against overcurrent, overtemperature, and undervoltage events.

VM undervoltage lockout

If at any time the voltage on the V M pin falls below the UVLO threshold voltage, V UVLO , all circuitry in the device is disabled, and all internal logic is reset. Operation resumes when V M rises above the UVLO threshold. The nFAULT pin is not driven low during an undervoltage condition.

Thermal shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. After the die temperature has fallen below the specified hysteresis (T_{HYS}), operation automatically resumes. The nFAULT pin is released after operation has resumed.

Overcurrent protection (OCP)

An analog current limit (I_{OCP}) circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time (t_{DEG}), all FETs in the H-bridge are disabled and the nFAULT pin is driven low. The driver is re-enabled after the OCP retry period (t_{OCP}) has passed. nFAULT becomes high again after the retry time. If the fault condition is still present, the cycle repeats. If the fault is no longer present, normal operation resumes and nFAULT remains deasserted. Note that only the H-bridge in which the OCP is detected will be disabled while the other bridge functions normally.

Overcurrent conditions are detected independently on both high-side and low-side devices; a short to ground, supply, or across the motor winding all result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, so it functions even without presence of the xISEN resistors.

Table 3. Device Protection

FAULT	CONDITION	H-BRIDGE	INTERNAL CIRCUIT	RECOVERY
VM undervoltage(UVLO)	V_M<2.4V	**Disabled**	**Disabled**	V_M>2.5V
Overcurrent(OCP)	I_{OUT}>I_{OCP}	**Disabled**	**Operating**	OCP
Thermal Shutdown(TSD)	T_J>T_{TSD}	**Disabled**	**Operating**	T_J<T_{TSD} − T_{HYS}

6.4 Device Functional Modes

The SC8833 is active unless the nSLEEP pin is brought logic low. In sleep mode, the H-bridge FETs are disabled (Hi-Z). Note that t_{SLEEP} must elapse after a falling edge on the nSLEEP pin before the device is in sleep mode.

The SC8833 is brought out of sleep mode automatically if nSLEEP is brought logic high. Note that t_{WAKE} must elapse before the outputs change state after wake-up

Table 3. Device Operating Modes

OPERATING MODE	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Operating	**nSLEEP high**	**Operating**	**Operating**
Sleep mode	**nSLEEP low**	**Disabled**	**Disabled**
Fault encountered	**Any fault condition met**	**Disabled**	**See Table3**

7 Application and Implementation

NOTE

Information in the following applications sections is not part of the SteadiChips Component specification, and SteadiChips does not warrant its accuracy or completeness. SteadiChips's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The SC8833 is used in stepper or brushed DC motor control. The following design procedure can be used to configure the SC8833 in a bipolar stepper motor application

7.2 Typical Application

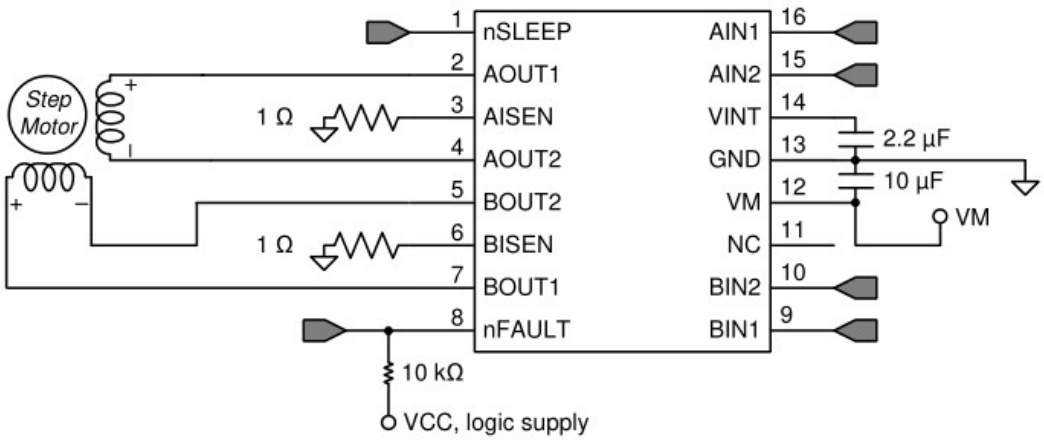


Figure 2. Schematic of SC8833 Application

8 Power Supply Recommendations

8.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor-drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power-supply capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless dc, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate size of bulk capacitor.

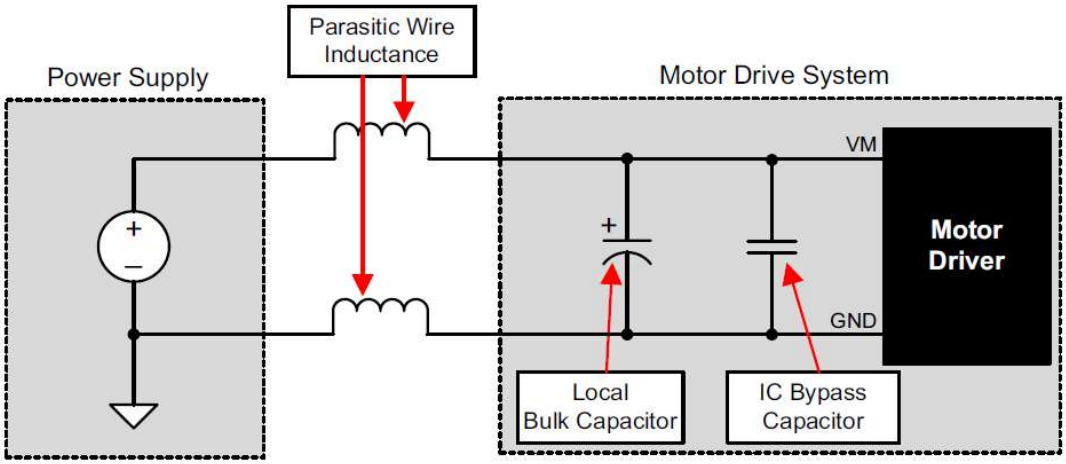


Figure 3. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply

9 Layout

9.1 Layout Guidelines

The VM and VCC pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1 µF rated for the VM and VCC supplies. These capacitors should be placed as close to the VM and VCC pins as possible with a thick trace or ground plane connection to the device GND pin. In addition bulk capacitance is required on the VM pin.

9.2 Layout Example

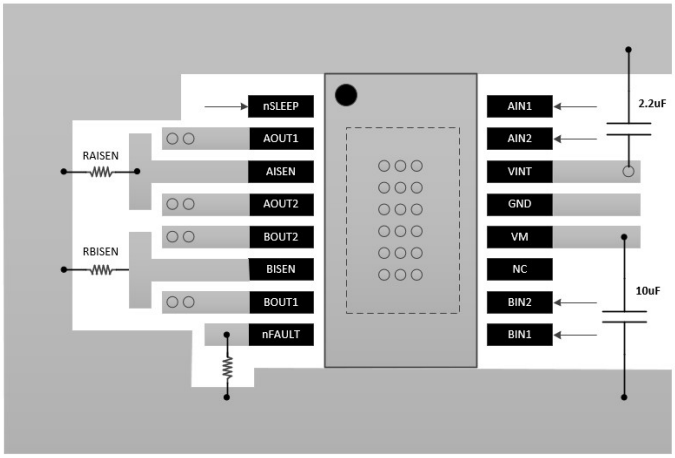


Figure 4. Simplified Layout Example

9.3 Power Dissipation

Power dissipation in the SC8833 is dominated by the power dissipated in the output FET resistance, or $R_{DS(on)}$. Average power dissipation when running both H-bridges can be roughly estimated by Equation 2:

$$P_{TOT} = 2 \times R_{DS(ON)} \times (I_{OUT(RMS)})^2 \quad (2)$$

where

- P_{TOT} is the total power dissipation
- $R_{DS(ON)}$ is the resistance of the HS plus LS FETs
- $I_{OUT(RMS)}$ is the RMS or DC output current being supplied to the load

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

NOTE

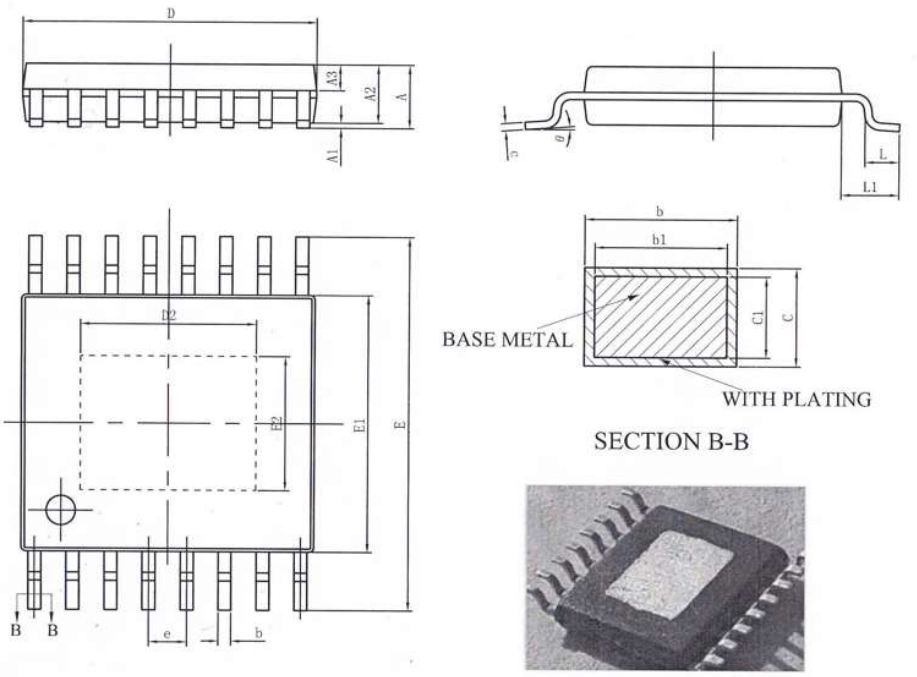
The value of $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases.

The SC8833 device has thermal shutdown protection. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10 Package Outline

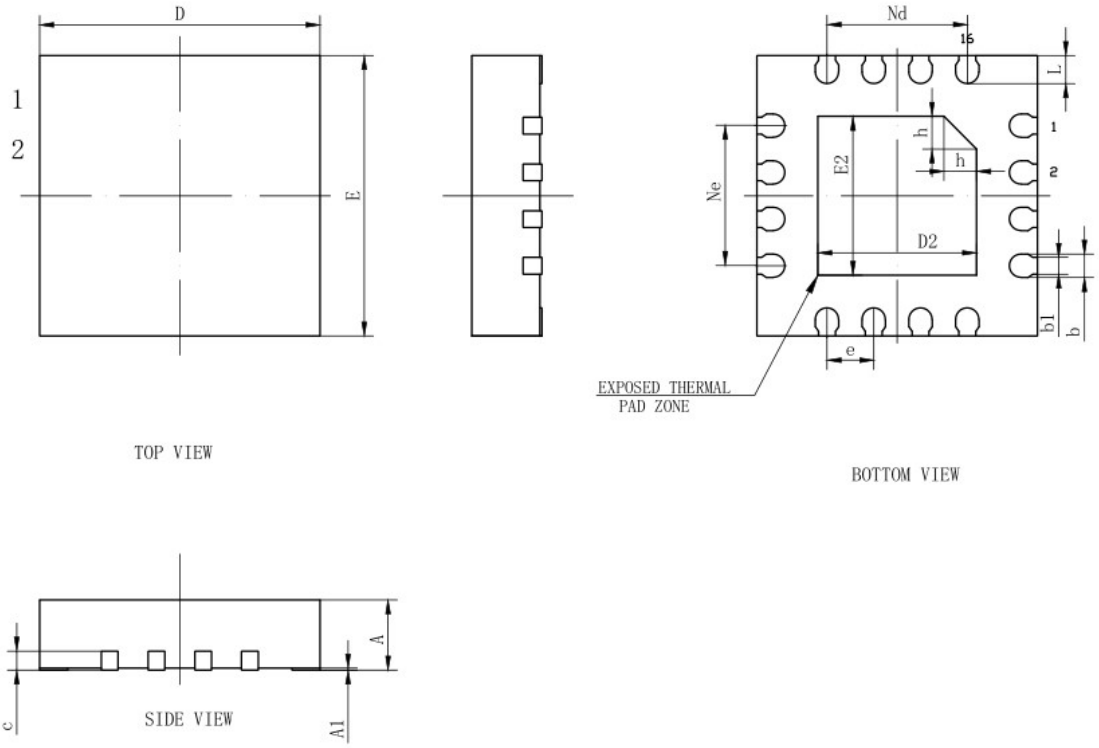
10.1 eTSSOP16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	—	0.75
L1	1.00BSC		
θ	0	—	8°

Size(mm) / L/F Size (mil)	D2	E2
91*118	2.80REF	2.10REF

10.2 QFN16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	0	0.02	0. 05
b	0. 18	0.25	0. 30
b1	0.18REF		
c	0.203REF		
D	2. 90	3. 00	3. 10
D2	1. 60	1. 70	1. 80
e	0. 50BSC		
Ne	1. 50BSC		
Nd	1. 50BSC		
E	2. 90	3. 00	3. 10
E2	1. 60	1. 70	1. 80
L	0. 25	0.30	0. 35
h	0. 30	0. 35	0. 40