Feature

- 2.7~5.5V power supply Voltage
- Chip available in MSOP-8 Package
- Low power dissipation: 15mA/17mA (3.3V/ 5V)

Comparator:

- 30ns propagation delay(@100mV Overdrive)
- Rail to Rail output, CMOS/TTL compatible
- Internal Hysteresis to ensure clean switching
- AC coupled input with 80mV level shift
- Offset voltage: +/-3mV Max
- Low HYS voltage temperature drift: 5uV/℃
- Low quiescent current: 251uA

Video Filter:

- 6th order 29MHz(-3dB) Butterworth HD video Filter
- 6 dB DC Gain & rail to rail output
- Can drive dual AC or DC coupled video channels (75Ω load)
- AC coupled Input with 230mV level shift

General Description

SC8341 is a low power dissipation, rail to rail output comparator and Video Filter on a single chip. The comparator apply a short 30ns propagation time at 100mV overdrive voltage; And the Video Filter apply attenuation -29dB @50MHz.

Input of SC8341 is AC-coupled for the comparator and filter; the internal clamper blocks apply 80mV level shift voltage for comparator and 230mV for LPF.

SC8341 comparator includes internal hysteresis to ensure clean output switch, and the HYS voltage has a ultra-low temperature drift 5uV/℃.

Applications

- HD Camera
- Threshold Detector /Discriminators;
- Sampling Circuits, IR Receivers;
- DVD video players, device of communication, Digital Set Top Box, etc.

Block Diagram

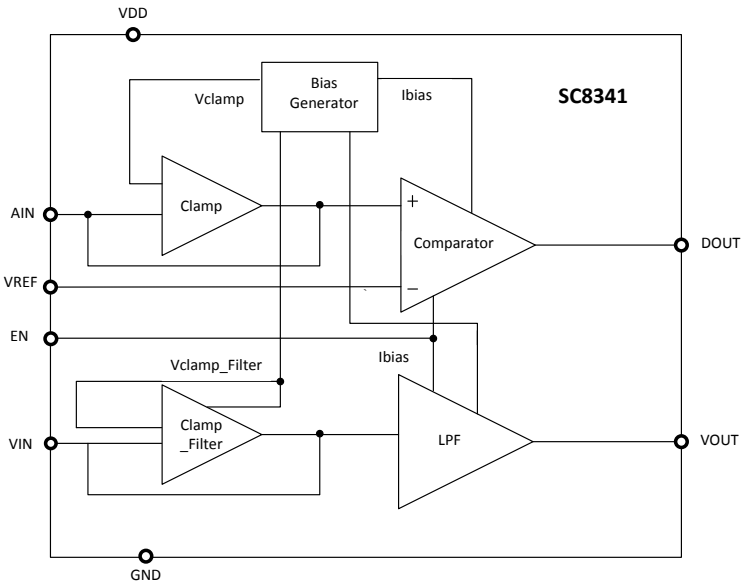


Fig.1 block diagram of SC8341

REV. 1.2

Absolute Maximum Ratings

(If out of these ratings, the filter may be fail or damaged)

Table 1

Symbol	Parameter	Rating	Units
VDD	Power supply	5.5	V
T_A	Operating ambient Temperature Range	-40~+85	℃
T_{STG}	Storage Temperature	-65~+150	℃

Recommended Operating Conditions

Table 2

Symbol	Parameter	Rating	Units
VDD	Power supply	2.7~5.5	V
T_A	Operating ambient Temperature Range	-40~+85	℃

Electrical Characteristics Video Filter Part

DC Characteristics

(Specifications are at RL=150ohm, Vin=1Vpp, Cin=0.1uF, output AC coupled cap=220uF, T=25 ºC, VDD =3.3V)

Table 3

Symbol	Parameter	Min	Typ	Max	Units
ICC	Total supply current (Vdd=3.3V)		15		mA
	Total supply current (Vdd=5V)		17		
I_Q	Quiescent current (Vdd=3.3V,No input& load)		12		mA
Isc	Output short to VDD(vin=VDD, Output to VDD)		72		mA
	Output short to GND(vin=VDD, Output 10ohm to GND)		85		mA
Vols	Output Level Shift Voltage (Vin=0V,no load, input referred)		234		mV
V_{OH}	Output Voltage High Swing (VDD=3.3V)		2.8		V
	Output Voltage High Swing (VDD=5V)		4.5		V
V_{OL}	Output Voltage Low Swing (VDD=3.3V/5V)		224		mV
AV	Output Voltage Gain		6		dB
Iclamp-up	Pull up clamp current		6		mA
Iclamp-down	Pull down clamp current		160		nA
PSRR	Power supply rejection ratio (f=50Hz)		58		dB
	Power supply rejection ratio (f=1MHz)		36		

AC Characteristics

(Specifications are at RL=150ohm, Vin=1Vpp, Cin=0.1uF, output AC coupled cap=220uF, T=25 ºC, VDD =3.3V)

Table 4

Symbol	Parameter	Min	Typ	Max	Unit
BW(-3 dB)	The Band width of -3dB		29		MHz
Att(f=50MHz)	Stop band Attenuation at 50MHz		-30		dB
Att(f=25MHz)	Stop band Attenuation at 25MHz		-1.0		dB
THD	Total Harmonic Distortion(25M ， 0.6Vpp)		-48		dB
SNR	Signal to Noise Ratio*1		64		dB
T_{GD}	Group Delay Variation [100k~21MHz]		8		ns
Rout	Output Impedance at f=10MHz		1		ohm
SR	Slow Rate (Vin=1Vpp, 20%~80%)		110		V/us

*1: White Signal, 100kHz~30MHz,SNR=20*Log(714mV/RMS noise)

Electrical Characteristics Comparator Part

(Specifications are at VDD=+2.7V ~ +5.5V, Cin=0.1uF, Vin-=1.2V, RL=10Kohm, CL=15pF, T=25 ºC)

Table 5

Symbol	Parameter		Min	Typ	Max	Units
VDD	Operating Supply Voltage		2.7	3.3	5.5	V
V_{OS}	Input Offset Voltage*1		-3	+/-0.15	+3	mV
V_{OS_TC}	Input Offset voltage Temp Drift		0.6	2.0	4.7	uV/℃
V_{hyst}	Input Hysteresis Voltage		3	5	10	mV
V_{hyst_TC}	Input Hysteresis Voltage Temp Drift			4.8	5.4	uV/℃
C_{IN}	Input Capacitance	Differential		1.8		pF
		Common Mode		3.6		
R_{IN}	Input Resistance			>100		GΩ
I_Q	Quiescent Current			251		uA
I_{SC}	Output short to VDD			25		mA
Vin_cm	Common mode Input voltage		GND+0.2	-	VDD-0.2	V
Vols	Output Level Shift Voltage (Vin=0V,no load, input referred)		70	80	90	mV
V_{OH}	Output Voltage High Swing		VDD-0.3			V
V_{OL}	Output Voltage Low Swing				GND+0.3	mV
Iclamp-up	Pull up clamp current			6.7		mA
Iclamp-down	Pull down clamp current			126		nA
CMRR	Common Mode Rejection Ratio			70		dB
PSRR	Power supply rejection ratio			63		dB
t_R	Rising time			3.5		ns
t_F	Falling time			2.8		ns
T_{PD+}	Propagation Delay(Low to High)			30		ns
T_{PD-}	Propagation Delay(High to Low)			28.5		ns
T_{PDSKEW}	Propagation Delay Skew*2			1.50		ns

*1: The input offset voltage is the average of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

*2: Propagation Delay Skew is defined as: T_{PD+}-T_{PD-}.

PAD Definition

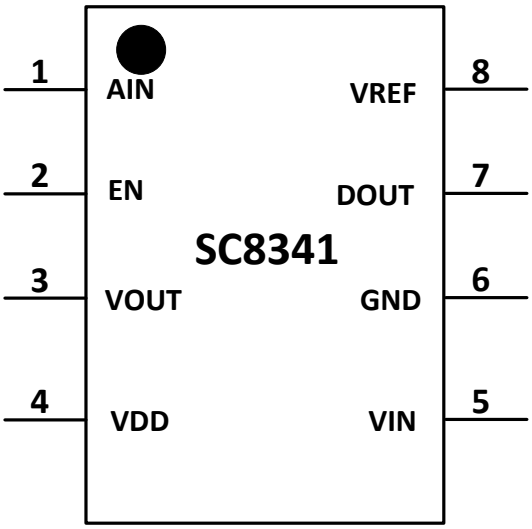


Fig.2 Pad definition of SC8341

Table 6 Pad definition

Pin	Name	I/O	Analog/Digital	Description
1	AIN	I	A	Input Signal PAD for Comparator
2	EN	I	A	The whole chip enable control pin, EN=high chip work; EN=low chip shut down;
3	VOUT	O	A	Video Filter output PAD
4	VDD	POWER	POWER	Power supply (3.3V/5V) ,connect to positive voltage supply
5	VIN	I	A	Video signal input PAD, AC coupled, Apply with 80mV Clamp up voltage
6	GND	GROUND	GROUND	Ground pin. Connect to the most negative supply, ALL GND pads are connected on die
7	DOUT	O	A	Comparator Output PAD, High Voltage level is Pulled to VDD, Low Voltage is GND
8	VREF	I	A	The DC reference voltage input PAD for comparator

Application Circuits

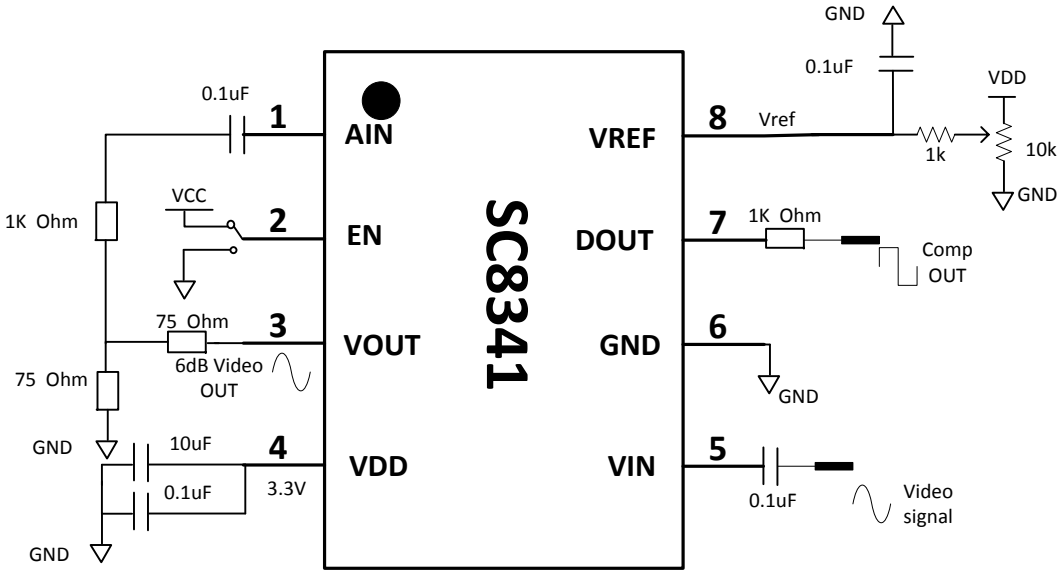
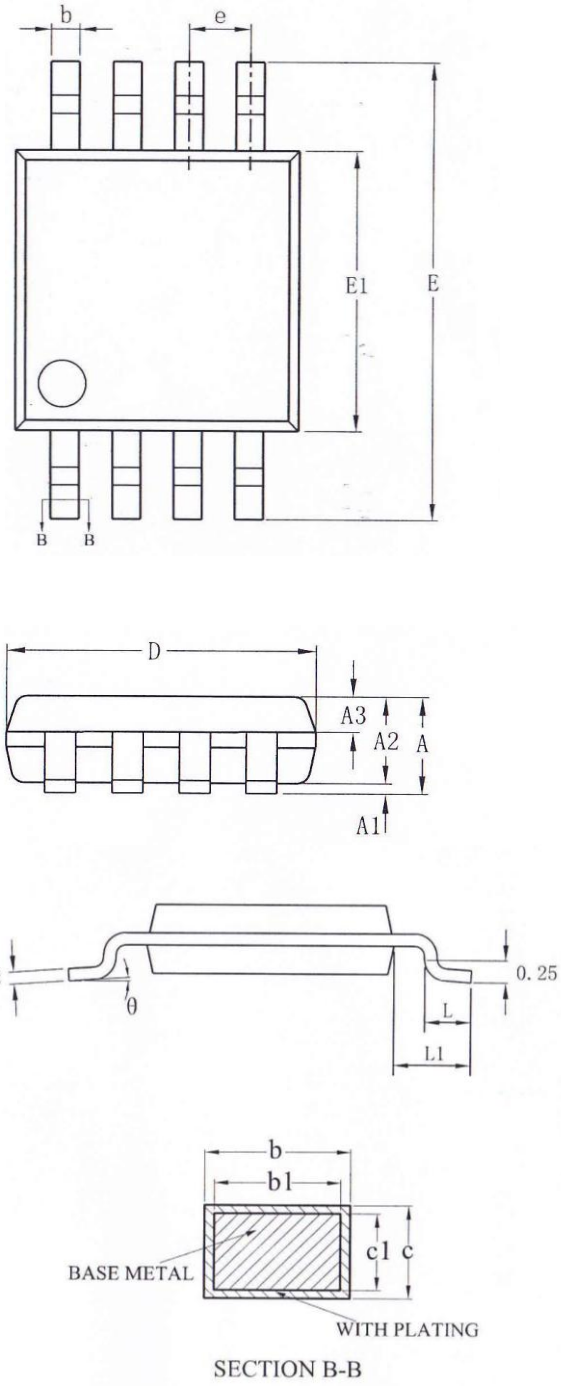


Fig.3 Applications Circuits of SC8341

Package

MSOP-8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	—	0.36
b1	0.27	0.30	0.33
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.40	—	0.70
L1	0.95REF		
θ	0	—	8°

Fig.4 Package of SC8341

Version History：

Ver.	Modify date	Modify Reason	Author	note
Initial(V1.0)	2017-02-21		wlli	
1.1	2017-03-01	Modify the application diagram	wlli	
1.2	2017-06-23	Modify the chip description on first page	wlli	