### Overcurrent protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than tDEG, all FETs in the H-bridge are disabled. Operation resumes automatically after tRETRY has elapsed. Overcurrent conditions are detected on both the high-side and low-side devices. A short to the VM pin, GND, or from the OUT1 pin to the OUT2 pin results in an overcurrent condition.

### Thermal shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature falls to a safe level, operation automatically resumes.

**Table 2. Fault Behavior**

| FAULT | CONDITION | H-BRIDGE | INTERNAL CIRCUIT | RECOVERY |
|---|---|---|---|---|
| **VCC undervoltage(UVLO)** | $V_{CC}$<1.5V | **Disabled** | **Disabled** | $V_{CC}$>1.6V |
| **Overcurrent(OCP)** | $I_{OUT}$>1.2A(MIN) | **Disabled** | **Operating** | $t_{OCR}$ |
| **Thermal Shutdown(TSD)** | $T_J$> • 0 , 1 | **Disabled** | **Operating** | $T_J$< • |

### 6.4 Device Functional Modes

The SC8837C device is active unless the nSLEEP pin is brought logic low. In sleep mode the H-bridge FETs are disabled Hi-Z. The SC8837C device is brought out of sleep mode automatically if nSLEEP is brought logic high.

The H-bridge outputs are disabled during undervoltage lockout, overcurrent, and overtemperature fault conditions.

**Table 3. Device Operating Modes**

| OPERATING MODE | CONDITION | H-BRIDGE | INTERNAL CIRCUITS |
|---|---|---|---|
| **Operating** | **nSLEEP high** | **Operating** | **Operating** |
| **Sleep mode** | **nSLEEP low** | **Disabled** | **Disabled** |
| **Fault encountered** | **Any fault condition met** | **Disabled** | **See Table2** |

## 7 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the SteadiChips Component specification, and SteadiChips does not warrant its accuracy or completeness. SteadiChips ¶ Vustomers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 7.1 Application Information

The SC8837C device is device is used to drive one DC motor or other devices like solenoids. The following design procedure can be used to configure the SC8837C device.

### 7.2 Typical Application

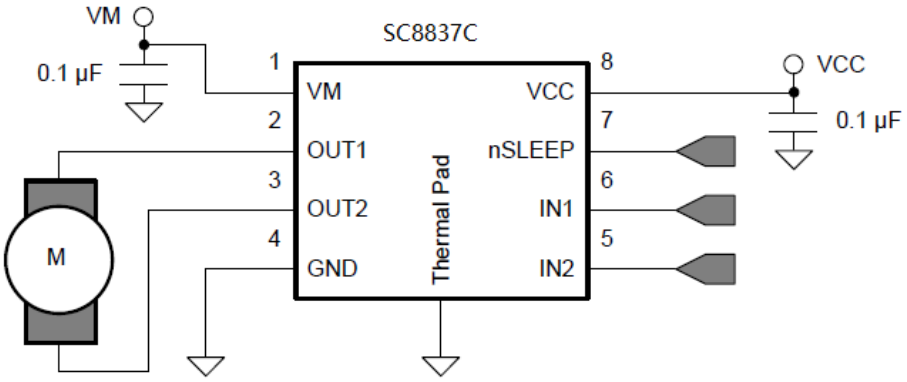



**Figure 2. Schematic of SC8837C Application**

## 8 Power Supply Recommendations

### 8.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor-drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

‡ The highest current required by the motor system
‡ The power-supply capacitance and ability to source current
‡ The amount of parasitic inductance between the power supply and motor system
‡ The acceptable voltage ripple
‡ The type of motor used (brushed dc, brushless dc, stepper)
‡ The motor braking method

The inductance between the power supply and motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate size of bulk capacitor.

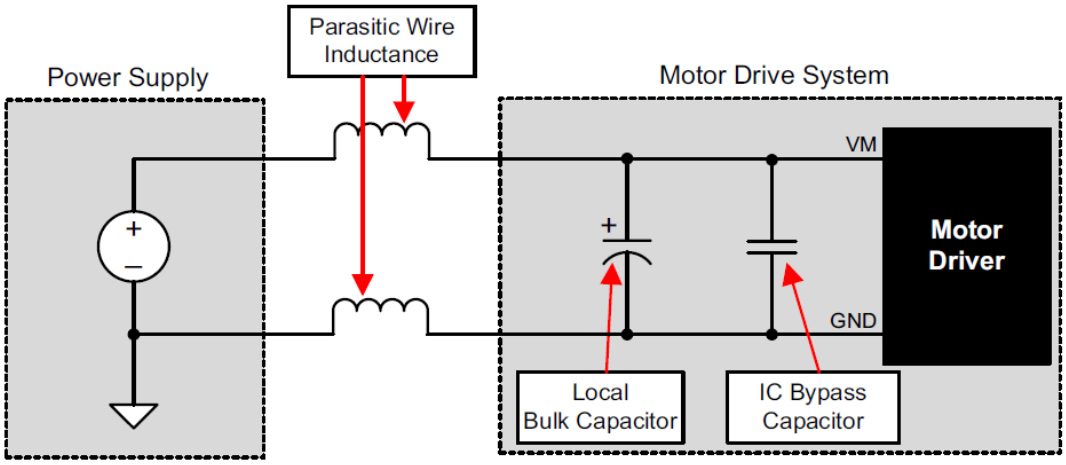



**Figure 3. Example Setup of Motor Drive System With External Power Supply**

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply

## 9 Layout

### 9.1 Layout Guidelines

The VM and VCC pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1 µF rated for the VM and VCC supplies. These capacitors should be placed as close to the VM and VCC pins as possible with a thick trace or ground plane connection to the device GND pin. In addition bulk capacitance is required on the VM pin.

### 9.2 Layout Example

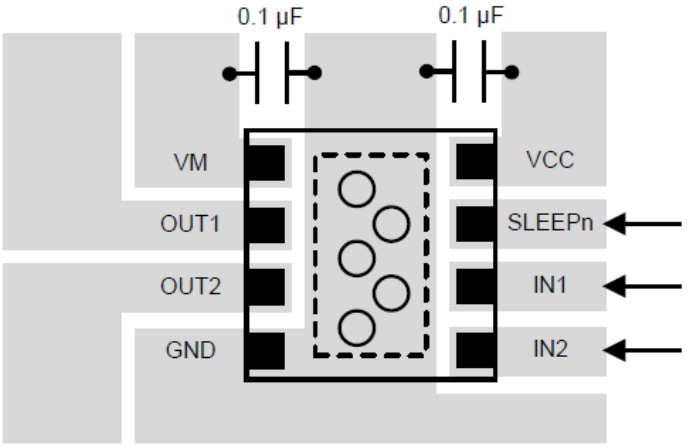



**Figure 4. Simplified Layout Example**

### 9.3 Power Dissipation

Power dissipation in the SC8837C is dominated by the power dissipated in the output FET resistance, or $R_{DS(on)}$. Average power dissipation when running both H-bridges can be roughly estimated by Equation 1:

$$P_{TOT} = R_{DS(ON)} \times (I_{OUT(RMS)})^2 \quad (1)$$

where

- $P_{TOT}$ is the total power dissipation
- $R_{DS(ON)}$ is the resistance of the HS plus LS FETs
- $I_{OUT(RMS)}$ is the RMS or DC output current being supplied to the load

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

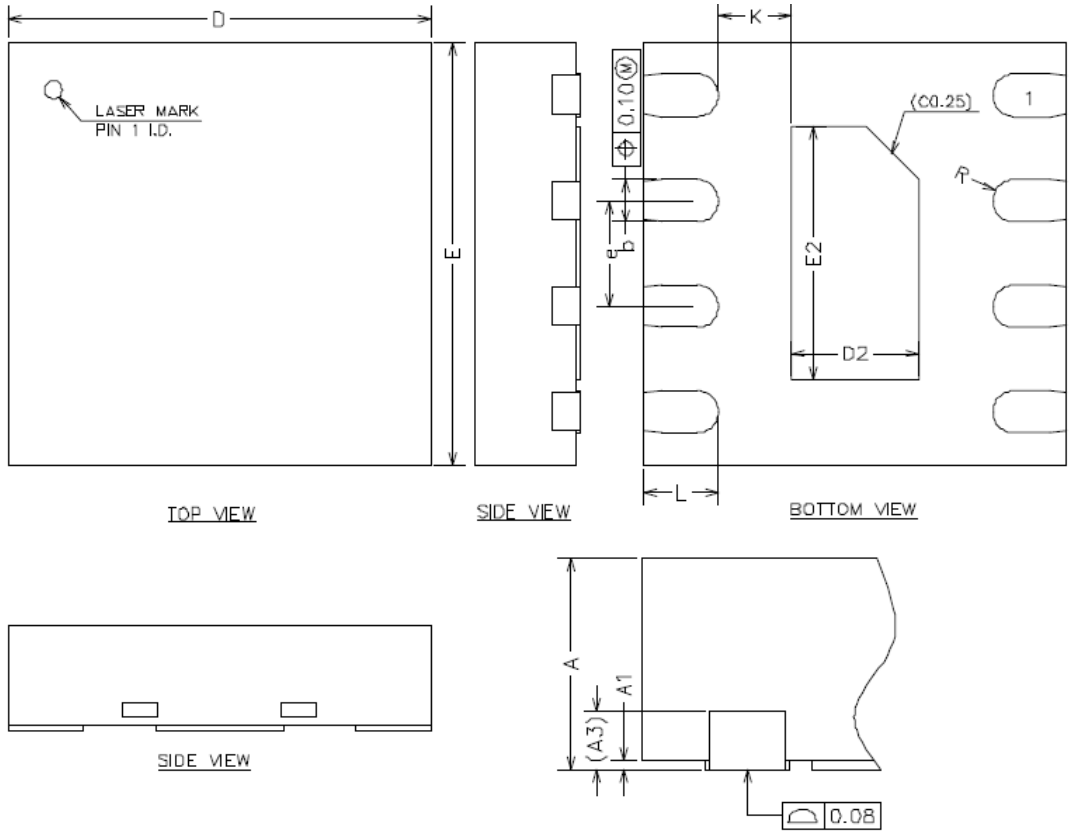
**NOTE**

The value of $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases.

The SC8837C device has thermal shutdown protection. If the die temperature exceeds approximately 150℃, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

## 10 Package Outline




COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | | 0.20REF | |
| b | 0.15 | 0.20 | 0.25 |
| D | 1.90 | 2.00 | 2.10 |
| E | 1.90 | 2.00 | 2.10 |
| D2 | 0.50 | 0.60 | 0.70 |
| E2 | 1.10 | 1.20 | 1.30 |
| e | 0.40 | 0.50 | 0.60 |
| K | 0.20 | — | — |
| L | 0.30 | 0.35 | 0.40 |
| R | 0.09 | — | — |