Motor Driver for camcorder and security-camera

1. Feature

- ❒ Voltage drive system 256-step microstep drivers (2 system)
- ❒ Super low noise Zoom or Focus driver
- ❒ 0.50-A Maximum drive current per H-bridge
- ❒ Motor control by 4-line serial data communication Built-in dc motor driver
- ❒ Built oscillation circuit, with external crystal
- ❒ 32 pin Plastic Quad Flat Non-leaded Package (QFN Type with thermal pad)

2. Applications

- ■ Camcorder
- ■ Security-camera
- ■ Robot
- ■ Precision industrial equipment

3. General Description

SC8929 is a lens motor driver IC for camcorder and security-camera featuring the functions of IR-cut control. Voltage drive system and several torque ripple correction techniques enable super- low noise micro step drive.

4. Package

Part Number	Package	Body Size
SC8929	QFN (32)	5.0mm x 5.0mm

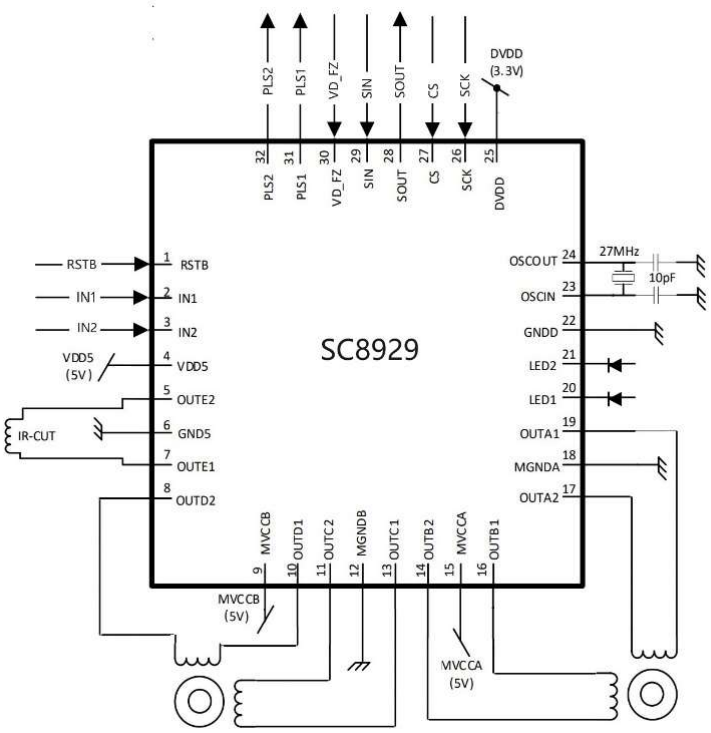


Fig.1 Simplified Application of SC8929

5. PAD Definition

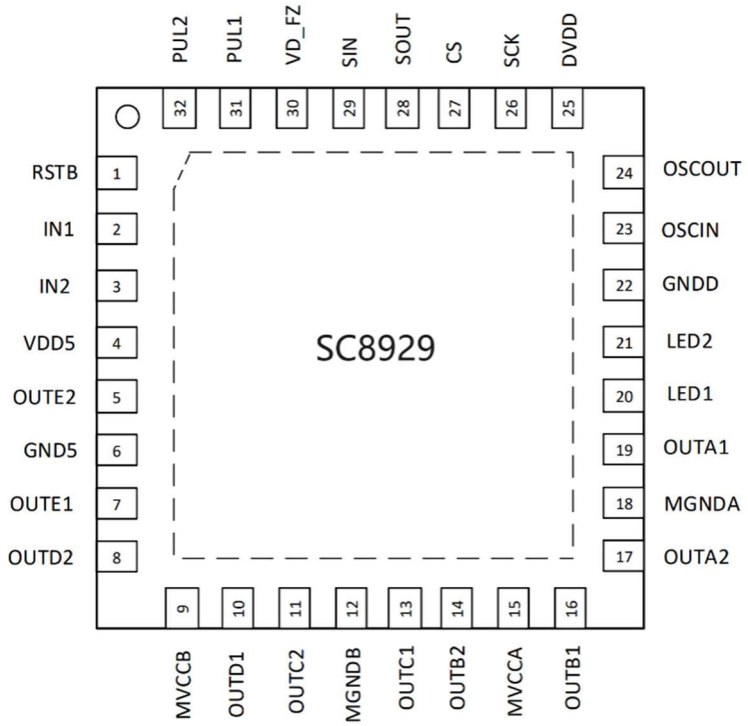


Fig.2 Pad definition of SC8929

Table 1 Pad Functions

Pin	Name	I/O	Description
1	RSTB	I	Reset signal input
2	IN1	I	Motor IN1 input
3	IN2	I	Motor IN2 input
4	VDD5	POWER	Power supply for motor E
5	OUTE2	O	Motor output E2
6	GND5	GROUND	GND for motor E
7	OUTE1	O	Motor output E1
8	OUTD2	O	Motor output D2
9	MVCCB	POWER	Power supply for motor B
10	OUTD1	O	Motor output D1
11	OUTC2	O	Motor output C2
12	MGNDB	GROUND	GND for motor B
13	OUTC1	O	Motor output C1
14	OUTB2	O	Motor output B2
15	MVCCA	POWER	Power supply for motor A
16	OUTB1	O	Motor output B1
17	OUTA2	O	Motor output A2
18	MGNDA	GROUND	GND for motor A

19	OUTA1	O	Motor output A1
20	LED1	I	Open-drain 1 for driving LED
21	LED2	I	Open-drain 2 for driving LED
22	GNDD	GROUND	Digital GND
23	OSCIN	I	OSCIN
24	OSCOUT	O	OSCOUT
25	DVDD	POWER	3 V digital power supply
26	SCK	I	Serial clock input
27	CS	I	Chip select signal input
28	SOUT	O	Serial data output
29	SIN	I	Serial data input
30	VD_FZ	I	Focus zoom sync. signal input
31	PLS1	O	Pulse 1 output
32	PLS2	O	Pulse 2 output

Absolute Maximum Ratings

(If out of these ratings, the filter may be failed or damaged)

Table 2

Symbol	Parameter	Min	Typ	Max	Unit	Note
DVDD	Controller supply voltage	-0.3		4.0	V	*1
MVCCA MVCCB	Supply voltage for motor controller 1	-0.3		5.5	V	*1
VDD5	Supply voltage for motor controller 2	-0.3		5.5	V	*1
Topr	Operating ambient temperature	-20		85	℃	*2, *4
T_j	Operating junction temperature	-20		125	℃	*2
Tstg	Storage temperature	-55		125	℃	*2
OUTA1, OUTA2 OUTB1, OUTB2 OUTC1, OUTC2 OUTD1, OUTD2	Motor driver 1 (focus, zoom) H bridge drive current (DC current)	-0.5		+0.5	A/ch	
OUTE1, OUTE2	Motor driver 2 (ir-cut) H bridge drive current (DC current)	-0.5		+0.5	A/ch	
IM(pulse)	Instantaneous H bridge drive current	-0.6		+0.6	A/ch	
Itotal(max)		-0.8		+0.8	A	
OSCIN CS, SCK, SIN VD_FZ, RSTB	Input Voltage Range	-0.3		DVDD3+0.3	V	*3
PLS1, PLS2, SOUT, OSCOUT	Output Voltage Range	-0.3		DVDD3+0.3	V	*3
LED1, LED2	Output Current Range		30		mA	

Notes):

This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guarantee as it is higher than our stated recommended operating range.

When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25°C.

*3: (DVDD + 0.3) V must not be exceeded 4.0 V.

*4: The power dissipation shown is the value at Ta = 85°C for the independent (unmounted) IC package without a heat sink.

6. Recommended Operating Conditions

Table 3

Symbol	Parameter	Min	Typ	Max	Unit	Note
MVCCB MVCCA VDD5	Supply voltage range	3.0	5.0	5.5	V	*1
DVDD		3.0	3.3	3.6	V	*1
VOSCIN VCS VSCK VSIN VVD_FZ VRSTB	Input Voltage Range	-0.3		DVDD+0.3	V	*2
VPLS2 VPLS1 VSOUT OSCOUT	Output Voltage Range	-0.3		DVDD+0.3	V	*2
IOUTE2 IOUTE1	Output Current Range	-0.50		+0.50		*1
IOUTD2 IOUTD1 IOUTC2 IOUTC1 IOUTB2 IOUTB1 IOUTA2 IOUTA1		-0.50		+0.50	A	*1
Ta^{OPT}	Operating ambient temperature	-40		100	℃	

Note:

*1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: (DVDD + 0.3) V must not be exceeded 4.0 V.

7. Electrical Characteristics

Table 4

VDD5 = MVCCB = 5.0 V, DVDD = 3.3 V Ta = 25℃±2℃

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Current circuit, Common circuit						
IOmdisable	MVCC supply current on reset	No load, no 27 MHz input		0	3.0	μA
Imenable	MVCC supply current on enable	Output open, No 27 MHz input	0.05	0.3	1.0	mA
Icc3reset	3V supply current on reset	No 27 MHz input		0	10.0	uA
Icc3enable	3V supply current on enable	Output open, No 27 MHz input	0.2	1	3	mA
Icc5reset	VDD5 supply current on reset	No 27 MHz input		0	3.0	μA
Icc5enable	VDD5 supply current on enable	Output open, No 27 MHz input	0.05	0.1	0.4	mA
Icc3standby	3V supply current on standby	Output open, 27 MHz input, reset=high	6	12	20	mA
Digital input / output						
Vin(H)	High-level input	RSTB	0.48x DVDD		DVDD+0.3	V
Vin(L)	Low-level input	RSTB	-0.3		0.2x DVDD	V
Vout(H):SDATA	SOUT High-level output	[SOUT] 1mA source	DVDD-0.5			V
Vout(L):SDATA	SOUT Low-level output	[SOUT] 1mA sink			0.5	V
Vout(H): MUX	PLS1 to 2 High-level output		0.9*VDD			V
Vout(L): MUX	PLS1 to 2 Low-level output				0.1*VDD	V
Rpullret	Input pull-down resistance	RSTB	50	100	200	KΩ
Motor driver 1 (focus, zoom)						
RonFZ	H bridge ON resistance	IM=100mA （High side + Low side）	1.3	1.5	1.9	Ω
IleakFZ	H bridge leak current				0.8	μA
LED driver						
RonLED	Output ON resistance	I=20mA, 5V cell		2.5		Ω
IleakIR	Output leak current				0.8	μA
Motor driver 2 (ir-cut) VDD5 = 5 V, RL = 20 Ω, TA = 25°C, unless otherwise noted						
Roncut	H bridge ON resistance	IM=300mA		2.5		Ω
Ileakcut	H bridge leak current				0.8	μA
tr	Rise time				188	ns
tf	Fall time				188	ns
td	Delay time from SPI in to OUTE on			25* TSCK		s

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Note
Serial port input							
Sclock	Serial clock		1		5	MHz	*1
T1	SCK low time		100			ns	*1
T2	SCK high time		100			ns	*1
T3	CS setup time		60			ns	*1
T4	CS hold time		60			ns	*1
T5	CS disable high time		100			ns	*1
T6	SIN setup time		50			ns	*1
T7	SIN hold time		50			ns	*1
T8	SOUT delay time				60	ns	*1
T9	SOUT hold time		60			ns	*1
T10	SOUT Enable-Hi-Z time				60	ns	*1
T11	SOUT Hi-Z-Enable time				60	ns	*1
Tsc	SOUT C load				40	pF	*1
Digital input / output							
VINH	High-level input threshold voltage	SCK, SIN, CS, VD_FZ		1.6		V	*1
VINL	Low-level input threshold voltage	SCK, SIN, CS, VD_FZ		1.02		V	*1
VOSC	OSCIN DC voltage	OSCIN floating,		1.7		V	*1
VOSCDC	OSCIN DC input coupling voltage		2.4			V	*1
VOSCAC	OSCIN AC input coupling voltage	CCOUP =0.1μF,	1.3			V	*1
FOSC	The frequency of crystal, Or External input		5		27	MHz	*1
Trst	RSTB signal pulse width		100			μs	*1
Vhysin	Input hysteresis width	SCK, SIN, CS, VD_FZ		0.34		V	*1
VDW	Video sync. signal width		80			μs	*1
T(VD-CS)	CS signal wait time 1		400			ns	*1
T(CS-DT1)	CS signal wait time 2		5			μs	*1

Note):

*1 Typical Value checked by design.

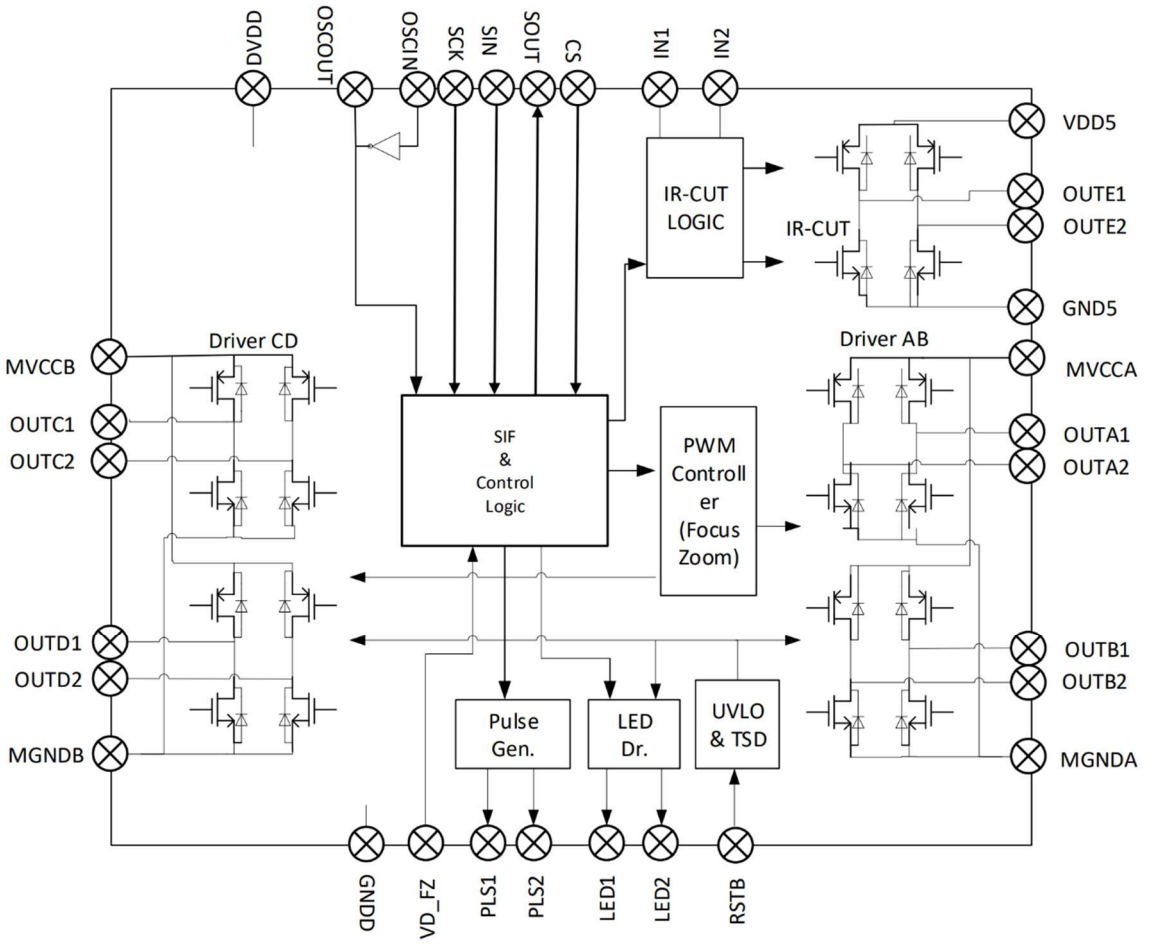
Electrical Characteristics (continued)

Symbol	Parameter	Condition	Limits			Unit	Note
			Min	Typ	Max		
Pulse generator							
PL1wait	Pulse start resolution for pulse 1	OSCIN = 27MHz		20.1		μs	*1
PL1width	Pulse resolution for pulse 1	OSCIN = 27MHz		1.20		μs	*1
PL2wait	Pulse start resolution for pulse 2	OSCIN = 27MHz		20.1		μs	*1
Thermal Shutdown							
Ttsd	Thermal shutdown operation temperature	Die temperature TJ		145		℃	*1
ΔT_{TSD}	Thermal shutdown hysteresis width			35		℃	*1
Supply voltage monitor circuit							
Vrston	3.3 V Reset operation			2.7		V	*1
Vrsthys	3.3 V Reset hysteresis			0.15		V	*1
VrstFZon	MVCCB Reset operation			2.5		V	*1
VrstFZhys	MVCCB Reset hysteresis			0.10		V	*1
VrstlSon	VDD5 Reset operation			2.5		V	*1
VrstlShys	VDD5 Reset hysteresis			0.10		V	*1

Note :

*1 Typical Value checked by design.

8. FUNCTIONAL BLOCK DIAGRAM



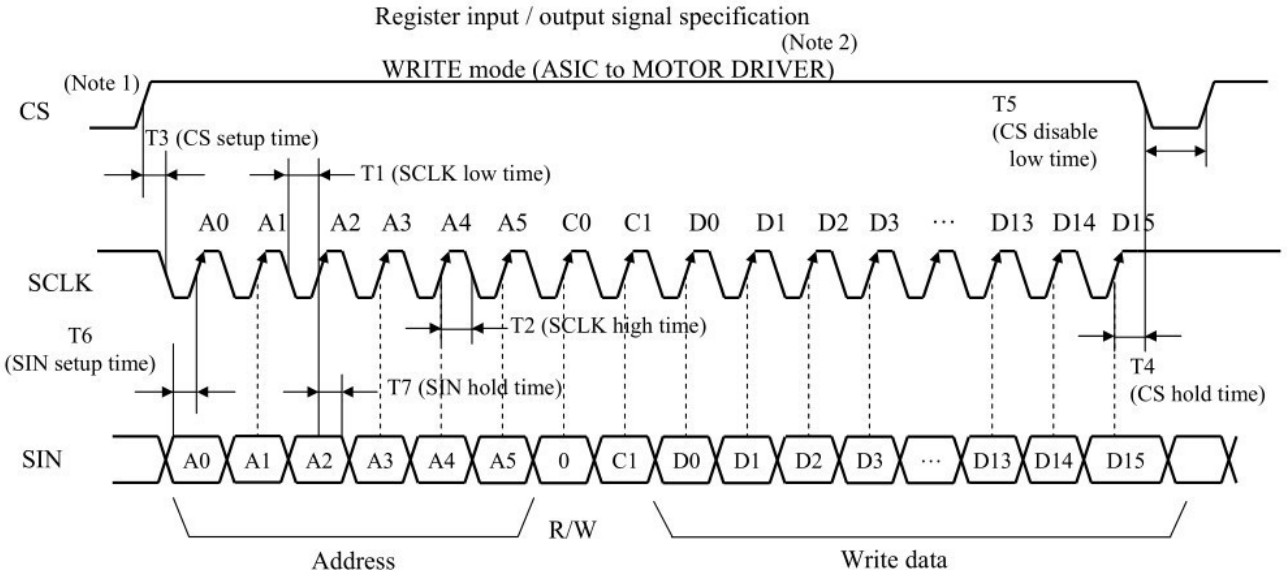
Note):

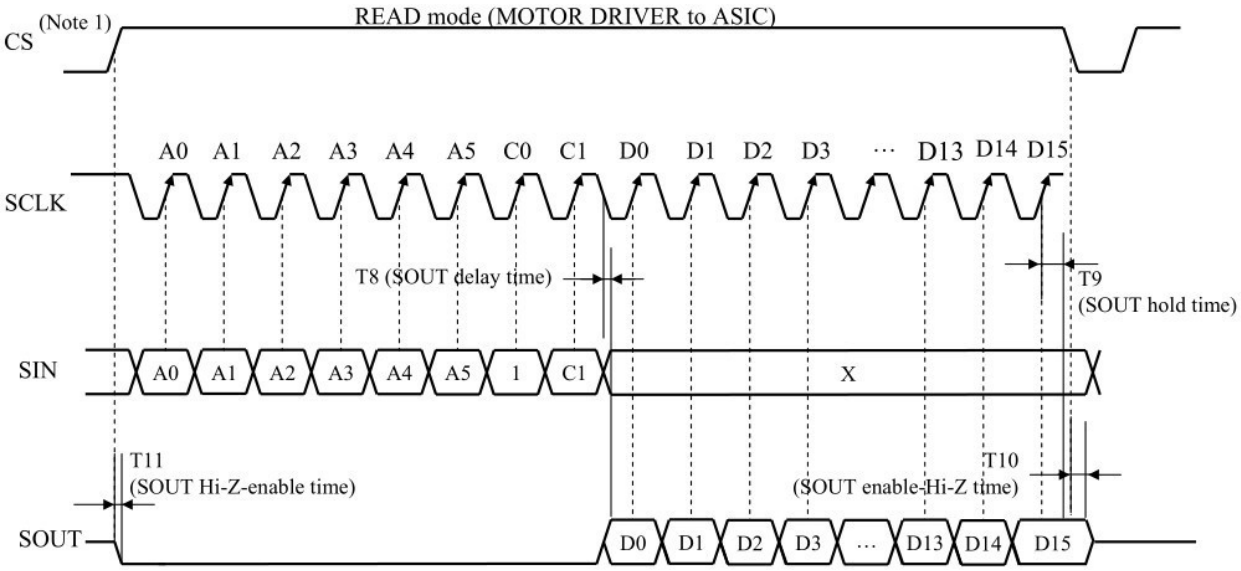
This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

9. Serial Interface

Timing Chart

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.





Notes):

1.CS default value of each cycle (Write / Read mode) starts from Low-level.

2.It is necessary to input the system clock OSCIN at write mode.

Electrical Characteristics (Reference values for design) at VDD5,MVCCx = 5.0 V, DVDD= 3.3 V

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
Sclock	Serial clock		1		5	MHz
T1	SCK low time		100			ns
T2	SCK high time		100			ns
T3	CS setup time		60			ns
T4	CS hold time		60			ns
T5	CS disable high time		100			ns
T6	SIN setup time		50			ns
T7	SIN hold time		50			ns
T8	SOUT delay time				60	ns
T9	SOUT hold time		60			ns
T10	SOUT Enable-Hi-Z time				60	ns
T11	SOUT Hi-Z-Enable time				60	ns
Tsc	SOUT C load				40	pF

Notes):

Ta = 25°C±2°C unless otherwise specified.

The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection. If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0BH	Reserved						MODESEL FZ	Reserved	TESTEN 1			Reserved				
20H		PWMRES [1:0]		PWMMODE [4:0]					DT1[7:0]							
21H									TESTEN2			FZTEST [4:0]				
22H			PHMODAB [5:0]						DT2A [7:0]							
23H	PPWB [7:0]								PPWA [7:0]							
24H			MICROAB [1:0]		LEDB	ENDISAB	BRAKEAB	CCWCWAB	PSUMAB [7:0]							
25H	INTCTAB [15:0]															
26H																
27H			PHMODCD [5:0]						DT2B [7:0]							
28H	PPWD [7:0]								PPWC [7:0]							
29H			MICROCD [1:0]		LEDA	ENDISCD	BRAKECD	CCWCWCD	PSUMCD [7:0]							
2AH	INTCTCD [15:0]															
2BH																
2C														INSWICH	IN1	IN2

❒ Register List

Address	Register name / Bit wide	Function
0Bh	TESTEN1	Test mode enable 1
	MODESEL_FZ	VD_FZ polarity selection
20h	DT1[7:0]	Start point wait time
	PWMMODE[4:0]	Micro step output PWM frequency
	PWMRES[1:0]	Micro step output PWM resolution
21h	FZTEST[4:0]	PLS1/2 pin output signal selection
	TESTEN2	Test mode enable 2
22h	DT2A[7:0]	α motor start point excitation wait time
	PHMODAB[5:0]	α motor phase correction
23h	PPWA[7:0]	Driver A peak pulse width
	PPWB[7:0]	Driver B peak pulse width
24h	PSUMAB[7:0]	α motor step count number
	CCWCWAB	αmotor rotation direction
	BRAKEAB	αmotor brake
	ENDISAB	αmotor enable/disable control
	LEDB	LED B output control
	MICROAB[1:0]	α motor sine wave division number
25h	INTCTAB[15:0]	αmotor step cycle
27h	DT2B[7:0]	β motor start point excitation wait time
	PHMODCD[5:0]	β motor phase correction
28h	PPWC[7:0]	Driver C peak pulse width
	PPWD[7:0]	Driver D peak pulse width
29h	PSUMCD[7:0]	β motor step count number
	CCWWCD	β motor rotation direction
	BRAKECD	β motor brake
	ENDISCD	β motor enable/disable control
	MICROCD[1:0]	β motor sine wave division number
2Ah	INTCTCD[15:0]	β motor step cycle
2Ch	INSWICH	DC Motor input mode select
	IN1	DC Motor input 1
	IN2	DC Motor input 2

All the SIF functions containing a data register are formatted at RSTB = 0.

□ Serial Interface Specifications

Data transfer starts at the rising edge of CS, and stops at the falling edge of CS.

One unit of data is 24 bits. (24 bits of the following format are called a data set in this book.)

Address and data are serially input from SIN pin in synchronization with the data clock SCK at CS = 1. Data is retrieved at the rising edge of SCK.

Moreover, data is output from SOUT pin at data readout. (Data is output at the rising edge of SCK.) SOUT outputs Hi-Z at CS = 0, and outputs "0" except data readout at CS = 1.

The control circuit of serial interface is reset at CS = 0.

❒ Data Format

0	1	2	3	4	5	6	7
A0	A1	A2	A3	A4	A5	C0	C1

8	9	10	11	12	13	14	15
D0	D1	D2	D3	D4	D5	D6	D7

16	17	18	19	20	21	22	23
D8	D9	D10	D11	D12	D13	D14	D15

C0: Register write / read selection 0: write mode, 1: read mode C1: Unused

A5 to A0: Address of register

D15 to D0: Data written in register

When C0 bit is "0", the write mode is selected. The address and data are retrieved from SIN in synchronization with the rising edge of data clock SCLK, and the data is stored in internal register in synchronization with the rising edge of CS.

SOUT outputs "0" in the write mode.

When the data which is 23 or less bits per 1 processing is received in the write mode, the received data becomes invalid.

The data of 25 or more bits is regarded as the continuous write mode, and the write operation is performed whenever the data of 24 bits is received. When the last data set is less than 24 bits in the continuous write mode, it becomes invalid. (The previous data set is valid.)

Even if noise occurs on SCK signal in the continuous write mode and the shifted data is received, pay attention to continue receiving or updating the shifted data.

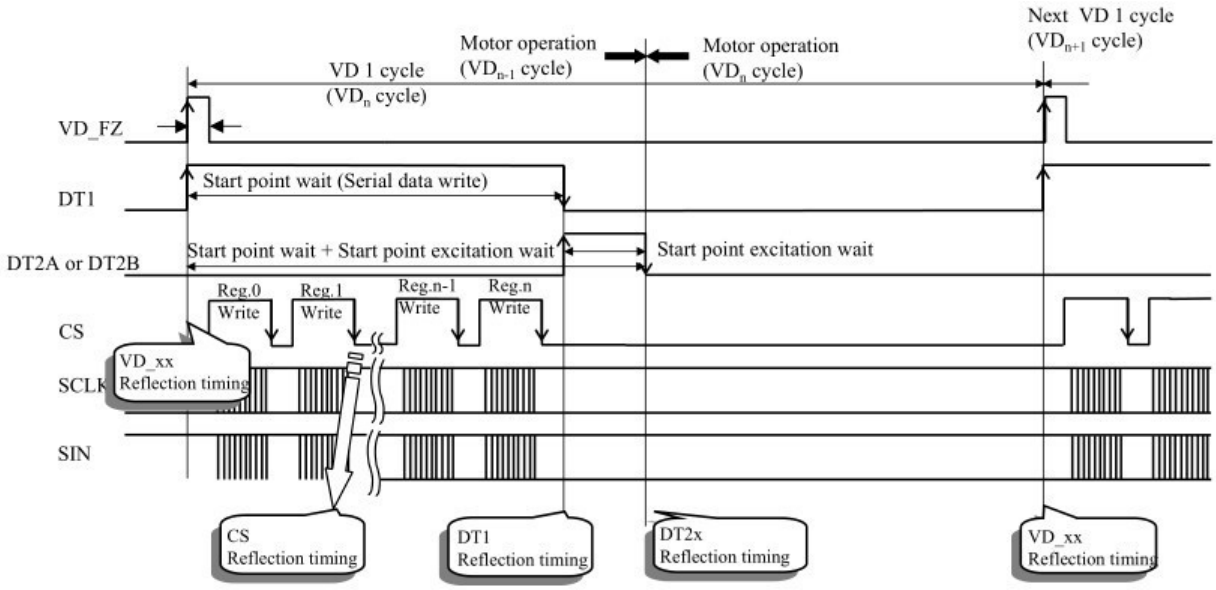
When C0 bit is "1", the read mode is selected. The address is retrieved from SIN in synchronization with the rising edge of SCK, and then the register value of the address specified is output as LSB first from SOUT, in synchronization with the rising edge of SCK.

When C0 bit is "1", the values of D15 to D0 of SIN do not be cared.

□ Formatting

All the SIF functions containing a data register are formatted at RSTB = 0.

❒ Register Setup Timing

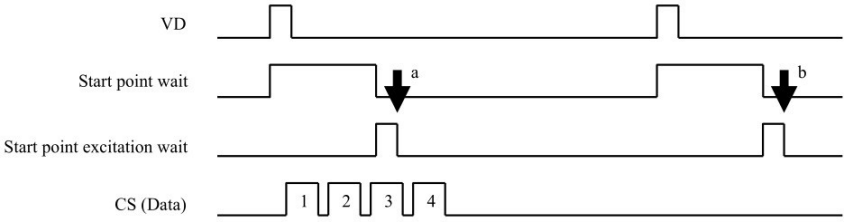


Address	Register Name	Setup Timing
0Bh	TESTEN1	CS
	MODESEL_FZ	CS
20h	DT1[7:0]	VD_FZ
	PWMMODE [4:0]	DT1
	PWMRES [1:0]	DT1
21h	FZTEST [4:0]	CS
	TESTEN2	CS
22h	DT2A [7:0]	DT1
	PHMODAB [5:0]	DT2A
23h	PPWA [7:0]	DT1
	PPWB [7:0]	DT1
24h	PSUMAB [7:0]	DT2A
	CCWCWAB	DT2A
	BRAKEAB	DT2A
	ENDISAB	DT1 or DT2A*
	LEDB	CS
	MICROAB [1:0]	DT2A
25h	INTCTAB [15:0]	DT2A
27h	DT2B[7:0]	DT1
	PHMODCD [5:0]	DT2B
28h	PPWC [7:0]	DT1
	PPWD [7:0]	DT1
29h	PSUMCD [7:0]	DT2B
	CCWWCD	DT2B
	BRAKECD	DT2B
	ENDISCD	DT1 or DT2B*
	LEDA	CS
	MICROCD [1:0]	DT2B
2Ah	INTCTCD [15:0]	DT2B
2Ch	INSWICH	CS
	IN1	CS
	IN2	CS

* 0 → 1: reflected at DT1 1 → 0: reflected at DT2x

In principle, the setup of registers for micro step should be performed during the interval of start point wait (Refer to the figure in page 17). The data which is written at timing except the interval of start point wait can be also received. However, if the write operation continues after the reflecting timing such as the end of start point excitation wait, the setup reflection timing may not be performed at the intended timing (Refer to the following figure). For example, if the data 1 to 4 which is updated at the end of start point excitation wait are written as the following figure, data 1 and 2 is updated at the timing a, and data 3 and 4 is updated at the timing b. Even if the data is written continuously like this, the update timing may be shifted to 1 VD.

Due to the above reason, the setup of registers should be performed during the interval of start point wait in order to reflect the updated content certainly.



10. VD signal internal processing

❒ Specifications

In this LSI, reflection timing and rotation timing of a stepping motor are based on the rising edge of VD_FZ respectively. The polarities of VD_FZ which are used for the internal processing can be set by the following setup.

❒ Register detail description

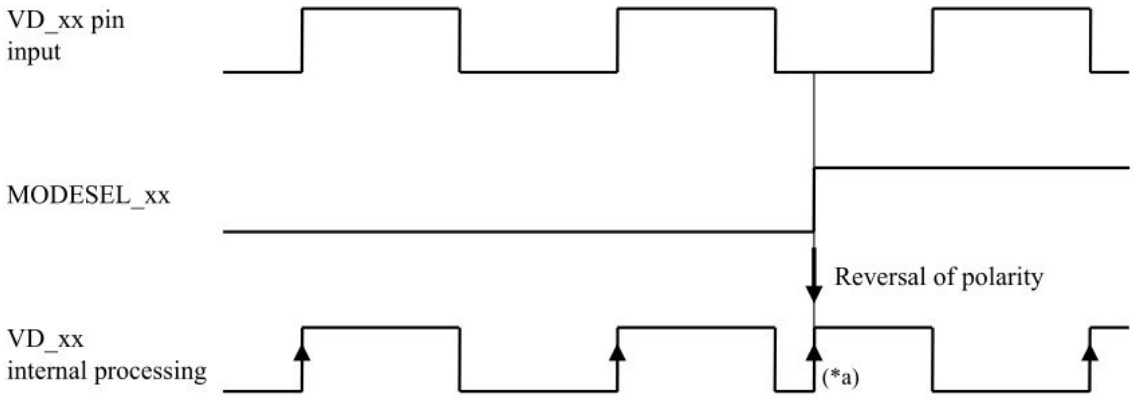
● MODESEL_FZ（VD_FZ polarity selection）

Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							MODESEL_FZ		Z						

MODESEL_FZ respectively set the polarities of VD_FZ signals which is input to this IC. When setting to "0", the polarity is based on the rising edge of VD_FZ inputted.
When setting to "1", the polarity is based on the falling edge of VD_FZ inputted

MODESEL_xx selects the polarity of VD_xx inputted. Therefore, depending on the selection timing of MODESEL_xx, the timing which is not related to the edge (*a) of VD_xx which is input as the following figure may be regarded as an edge.

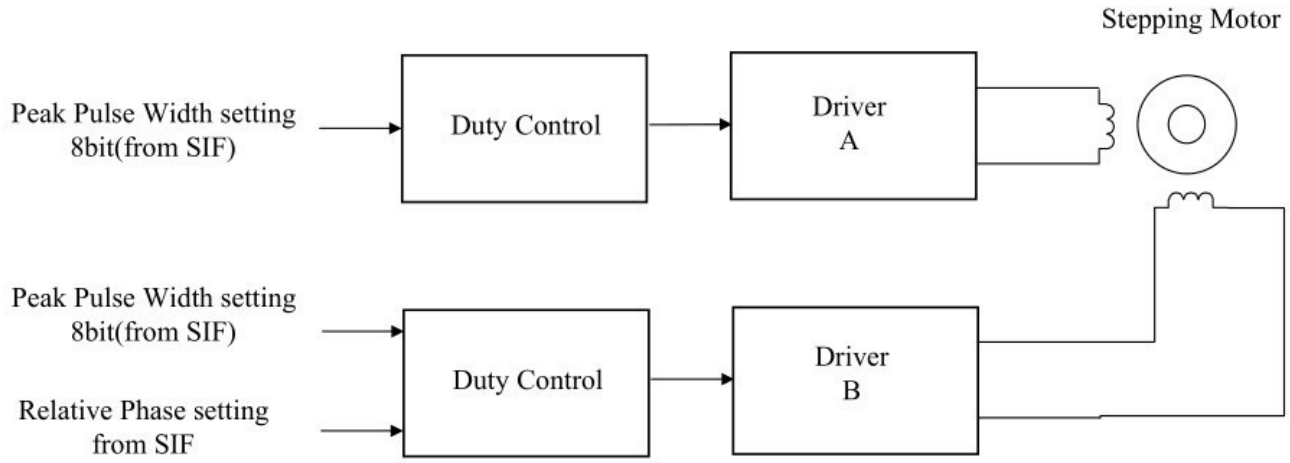
Setup value	VD polarity
0	Non-inverting
1	Inverting



Based on the rising edge of VD_xx internal processing

11. Micro Stepping Motor Driver

❒ Block Diagram



❒ This block is a stepping motor driver for focus and zoom, and the following setup can be performed by serial control. (The following description is for α motor: driver A/B. β motor: driver C/D is the same function as α motor.)

❒ Main setup parameters

1) Phase correction: The phase difference between a driver A and a driver B is on the basis of 90 degree, and can be adjusted from –22.5 degree to +21.8 degree. PHMODAB[5:0]
2) Amplitude correction: It is possible to set the load current of driver A/B independently. PPWA[7:0], PPWB[7:0]
3) PWM frequency: PWM driver chopping frequency is set. PWMMODE[4:0], PWMRES[1:0]
4) Quasi-sine wave: Number of divisions can be set to 64, 128 and 256. MICROAB[1:0]
5) Stepping cycle: Motor rotation speed is set. The rotation speed is constant regardless of number of divisions of quasi-sine wave. INTCTAB[15:0]

❒ Electrical Characteristics at VDD5, MVCCx = 5.0 V, DVDD, DVDD = 3.3 V

Notes) Ta = 25°C±2°C unless otherwise specified.

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
Motor driver 1 (focus, zoom)						
RonFZ	H bridge ON resistance	IM=100mA	1.3	1.5	1.9	Ω
IleakFZ	H bridge leak current				0.8	μA

❒ Setup Timing for Each Setup

Setup timing and number of times are shown as follows. Since the setups for address 27h to 2Ah are the same as those of 22h to 25h, the descriptions for address 27h to 2Ah are omitted. If each setup is set once, the setup is reflected at every VD pulses. Therefore, when the same setup is performed at two or more VD pulses, it is unnecessary to write at every VD pulse.

DT1[7:0] (Start point wait, Address 20h)
Update timing is set. After hard reset release (RSTB: Low → High), this setup should be performed before starting to excite and drive a motor. Since this setup is updated by the start of VD, it is unnecessary to write during the start point wait.

PWMMODE [4:0], PWMRES[1:0] (Micro step output PWM frequency setup, Address 20h)

Micro step output PWM frequency is set. After hard reset release (RSTB: Low to High), this setup should be performed before starting to excite and drive a motor (DT1 ends).

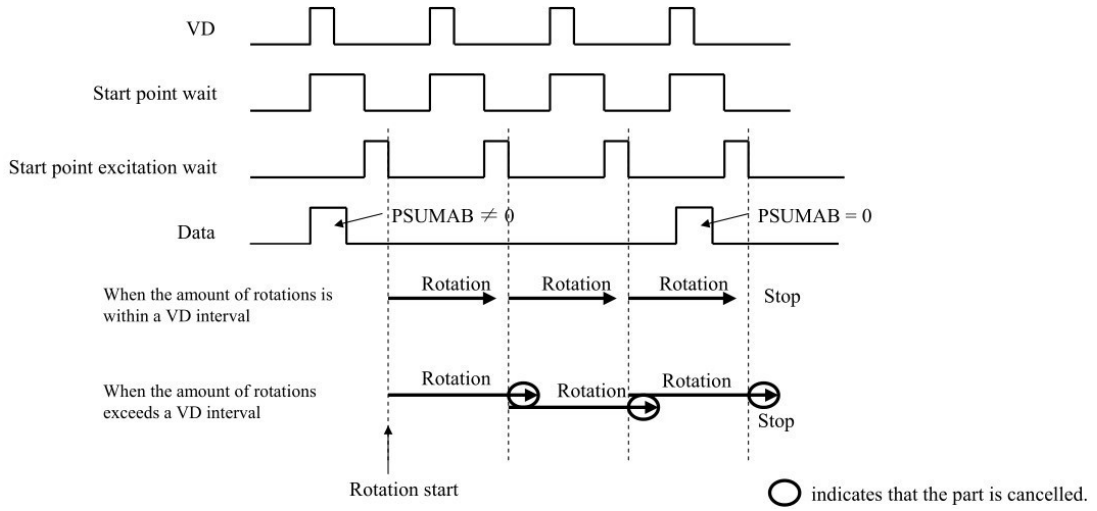
DT2A [7:0] (Start point excitation wait, Address 22h)
Updated timing is set. After hard reset release (RSTB: Low → High), this setup should be performed before starting to excite and drive a motor (DT1 ends).

PHMODAB [5:0] (Phase correction, Address 22h)
The correlation phase difference between coil A and B is corrected, and the driving noise is reduced. Since the amount of suitable phase correction depends on the rotation direction or rotation speed, the change of this setup should be performed simultaneously with the changes of the rotations direction (CCWCWAB) or rotation speed (INTCTAB), or it should be performed when a motor does not rotate.

PPWA [7:0], PPWB [7:0] (Peak pulse width, Address 23h)

PWM maximum duty is set. This setup should be performed before starting to excite and drive a motor (DT1 ends).

PSUMAB [7:0] (Step count number, Address 24h)
The amount of motor rotations in 1 VD interval is set. Every time VD pulse is input, the motor keeps rotating depending on the amount of rotations. Therefore, set to "0" in order to stop rotation of the motor. When the amount of rotations which exceeds 1 VD interval is set, the amount of rotations of a part which exceeds 1 VD interval is cancelled.



❒ Setup Timing of Each Setup (continued)

CCWCWAB (Rotation direction, Address 24h)
Rotation direction is set. This setup should be performed just before switching the rotation direction.

BRAKEAB (Brake setup, Address 24h)
A current is set to 0 by braking. Since it becomes impossible to get the excitation position of a motor by braking, this setup should not be performed except for the case of stopping immediately.

ENDISAB (Motor enable/disable setup, Address 24h)
Enable of a motor is set. Since a motor pin is Hi-Z when it is set to "Disable", do not set to "Disable" while a motor keeps rotating.

LEDA (LED setup, Address 24h)
LED ON/OFF is set. The setup is performed at the falling edge of CS.
(It is understood that it is not related to driving a motor. It is possible to turn ON/OFF independently.)

MICROAB [1:0] (Number of sine wave divisions, Address 24h)
Number of sine wave divisions is set. Even if this setup is changed, the amount of rotations and rotation speed do not vary.
If only the control which the number of divisions varies depending on the rotation speed is not performed, the problem dose not occur if it is set once after hard reset release (RSTB: Low → High).

INTCTAB [15:0] (Pulse cycle, Address 25h)
Pulse cycle is set. Rotation speed is determined by this setup.

❒ How to adjust register setting for micro stepping motor driver

In order to control lens, it is required to set motor rotation speed and amount of rotation per VD. Register settings relating to speed and amount of rotation are:

INTCTxx [15:0]: set time of each step (that is, the rotation speed) PSUMxx [7:0]: amount of rotation per VD period
When driving the motor continuously for several VD period, it is best to match rotation time (per VD) to VD period.

Below is a method to calculate INTCTxx [15:0] and PSUMxx [7:0] for smooth motor rotation.

Calculate INTCTxx [15:0] from desired rotation speed.

INTCTxx [15:0] × 768 = OSCIN frequency / rotation frequency

Calculate PSUMxx [7:0] from INTCTxx [15:0]. Round off if the result of PSUMxx [7:0] is not integer.
When the below equation is satisfied, the rotation time is equal to VD period, and smooth rotation is realized.

INTCTxx [15:0] × PSUMxx [7:0] × 24 = OSCIN frequency / VD frequency

If PSUMxx [7:0] is rounded off, recalculate INTCTxx [15:0] from the equation in 2).

Example) OSCIN frequency = 27 MHz, VD frequency = 60 Hz
Calculate PSUMxx [7:0] and INTCTxx [15:0] to rotate motor at 800 pps (1-2 phase). 800 pps = 100 Hz, so from equation in 1),

INTCTxx[15: GD30DR8300] = 27 MHz / (100 Hz × 768) = 352

Next, calculate PSUMxx [7:0] from equation in 2):

PSUMxx[7:0] = 1/(60 Hz) × 27 MHz / (352 × 24) = 53

Since PSUMxx [7:0] is rounded off, recalculate INTCTxx[15:0] from equation in 2):

INTCTxx [15:0] = 1/(60 Hz) × 27 MHz / (53 × 24) = 354

Refer to pages 23 and 28 for detail of PSUMxx[7:0] and INTCTxx[15:0].

If the value of left-hand side in 2) is smaller than right-hand side, the rotation time will be shorter than VD period and will cause discontinuous rotation. If left-hand side is smaller, the rotation time that exceeds 1 VD will be cancelled.

❒ Detail descriptions of register

● DT1[7:0]（Start point wait time）

Address			20h			Initial Value			0Ah						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT1[7:0]							

DT1[7:0] sets the delay time (start point wait time) until the data written in the serial data communication sends to the output.

It becomes possible to excite a motor after a start point wait switches "1" to "0". The start point wait starts to count after the rising edge of video sync signal (VD_FZ).

Since start point wait time is the trigger required for data acquisition, be sure to set to other than "0". When the value of register is "0", the data cannot be updated.

Refer to page 10 for the relationship of VD_FZ and start point wait time.

DT1	Start point wait
0	Prohibition
1	303.4us
255	77.4ms
n	n X 8192/27MHz

● DT2A[7:0]（Start point excitation wait α motor）

Address			22h			Initial Value		03h							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT2A[7:0]							

● DT2B[7:0]（Start point excitation wait β motor）

Address			27h			Initial Value		03h							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT2B[7:0]							

DT2A[7:0] and DT2B[7:0] set the delay time (start point excitation wait) until α motor and β motor start rotation. Motor rotation starts after start point excitation wait switches "1" to "0". The start point excitation wait starts to count after the falling edge of start point wait.

Since the falling edge is the trigger pulse which is required for data acquisition, be sure to input the data of other than "0". When the value of register is "0", the data cannot be updated.

Refer to page 17 for the relationship of VD_FZ and start point excitation wait time.

Setup value	Start point excitation wait
0	Prohibition
1	303.4us
255	77.4ms
n	n X 8192/27MHz

● PWMMODE[4:0]（Micro step output PWM frequency）

Address			20h			Initial Value			1Ch						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			PWMMODE[4:0]												

● PWMRES[1:0]（Micro step output PWM frequency resolution）

Address			20h			Initial Value			1h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	PWMRES														

PWMMODE [4:0] sets the frequency division value of system clock, OSCIN, which is used as the standard of PWM signal for micro step output. PWMMODE [4:0] can set in the range from 1 to 31.

PWM frequency at PWMMODE = 0 is the same as that at PWMMODE = 1.

PWMRES [1:0] sets the resolution of frequency division value set by PWMMODE [4:0]. PWM frequency is calculated by the following formula.

$$\text{PWM frequency} = \text{OSCIN frequency} / ((\text{PWMMODE} \times 2^3) \times 2^{\text{PWMRES}})$$

Refer to next part for the specific PWM frequency set by PWMMODE [4:0] and PWMRES [1:0] at OSCIN = 27MHz..

❒ PWM frequency setup

PWM frequency for OSCIN = 27 MHz is shown in below table.

PWMMODE	PWMRES			PWMMODE	PWMRES		
	0	1	2		0	1	2
1	3375.0	1687.5	843.8	17	198.5	99.3	49.6
2	1687.5	843.8	421.9	18	187.5	93.8	46.9
3	1125.0	526.5	281.3	19	177.6	88.8	44.4
4	843.8	421.9	210.9	20	168.8	84.4	42.2
5	675.0	337.5	168.8	21	160.7	80.4	40.2
6	526.5	281.3	140.6	22	153.4	76.7	38.4
7	482.1	241.1	120.5	23	146.7	73.4	36.7
8	421.9	210.9	105.5	24	140.6	70.3	35.2
9	375.0	187.5	93.8	25	135.0	67.5	33.8
10	337.5	168.8	84.4	26	129.8	64.9	32.5
11	306.8	153.4	76.7	27	125.0	62.5	31.3
12	281.3	140.6	70.3	28	120.5	60.3	30.1
13	259.6	129.8	64.9	29	116.4	58.2	29.1
14	241.1	120.5	60.3	30	112.5	56.3	28.1
15	225.0	112.5	56.3	31	108.9	54.4	27.2
16	210.9	105.5	52.7				

❒ Detail descriptions of register (continued)

● PHMODAB[5:0]（Phase correction α motor）

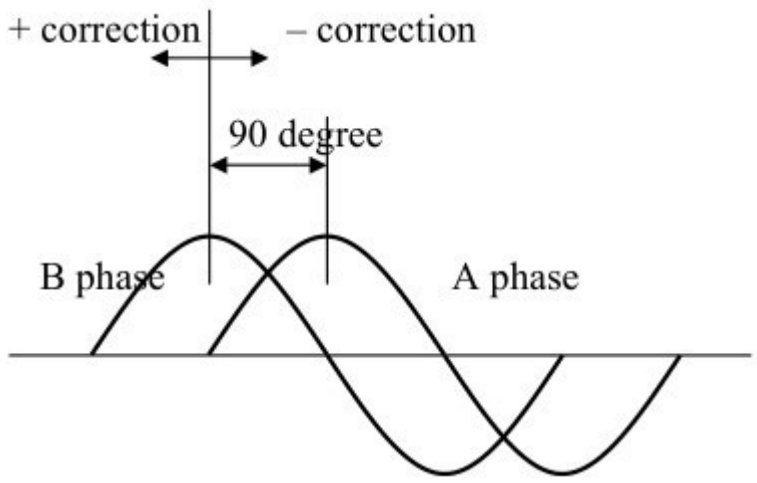
Address			22h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		PHMODAB [5:0]													

● PHMODCD[5:0] (Phase correction β motor)

Address			27h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		PHMODCD [5:0]													

Current phase differences of α motor and β motor shifts from 90 degree by PHMODAB[5:0] and PHMODCD[5:0] respectively. Setup resolution is 0.7 degree, and data is set in two's complement.

PHMODCD	Amount of phase correction
000000	±0°
000001	+0.7°
011111	+21.80°
100000	-22.50°
111111	-0.7°
Resolution	360°/512=0.7°



Stepping motor is configured so that phase difference between coils becomes 90 degree. However, the phase difference may shift from 90 degree due to the variation of a motor.

Therefore, even if phase difference in current waveform is exactly 90 degree, driving noise may occur due to the occurrence of rotation torque ripple.

This setup is for reducing the torque ripple which is occurred by the variation of a motor.

❒ Detail descriptions of register (continued)

- PPWA [7:0] （Driver A peak pulse width）
- PPWB [7:0] （Driver B peak pulse width）

Address			23h			Initial Value			0,0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PPWA [7:0]									PPWB [7:0]						

- PPWC [7:0] (Driver C peak pulse width)
- PPWD [7:0] (Driver D peak pulse width)

Address			28h			Initial Value			0,0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PPWC [7:0]									PPWD [7:0]						

PPWA[7:0] to PPWD[7:0] set the maximum duty of PWM at the position which the currents in driver A to

D are peak value respectively. The maximum duty is calculated by the following formula.

Driver X Maximum duty = PPWx / (PWMMODE

×8) When PPWx = 0 is set, coil current becomes 0.

Refer to page 34 for the operation at the time when the duty exceeding 100% is set.

Example) When PPWA [7:0] = 200, PWMMODE [4:0] = 28 is set, maximum duty of driver A will be

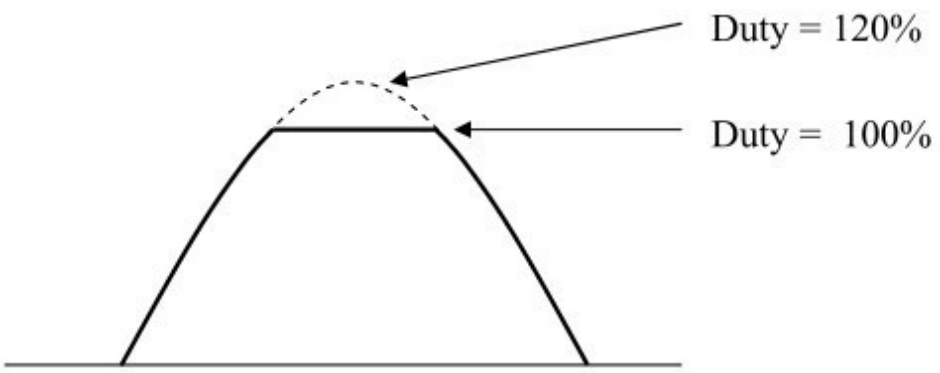
200 / (28 × 8) = 0.89

Maximum duty may exceed 100% depending on the setup values of PWMMODE and PPWx.

Since the duty does not certainly exceed 100% at PWM operation in this case, the peak point of sine wave (current waveform) becomes flat as follows.

Example 1 ）When PWMMODE＝10, PPWx＝96, Maximum duty = 96 / (10 × 8) ＝

120% The target current waveform is indicated as the following full line.



❒ Detail descriptions of register (continued)

● PSUMAB [7:0] (α motor step count number)

Address			24h			Initial Value		0							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								PSUMAB [7:0]							

● PSUMCD [7:0] (β motor step count number)

Address			29h			Initial Value		0							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								PSUMCD [7:0]							

PSUMAB [7:0] and PSUMCD [7:0] set the number of step counts of α motor and β motor respectively.

Since the number of setup step counts is converted to 256-step inside, the amount of rotation becomes the same regardless of the number of divisions.

To stop the rotation of a motor, set PSUMxx [7:0] = 0.

Setting value	Number of steps		
	64-step conversion	128-step conversion	256-step conversion
0	0	0	0
1	2	4	8
255	510	1020	2040
n	2n	4n	8n

If maximum duty is set to other than "0" at PSUMxx [7:0] = 0, the position is held in the state of excitation.

If a motor can hold the position by cogging torque without motor current, the position is held even if the maximum duty is set to 0.

Example) When PSUMAB [7:0] = 8 is set, the amount of rotation is 16 steps (64-step conversion).

This is 16/64 =1/4 of a sine wave. The amount of rotation becomes 1/4 of a sine wave also in 128 and 256-step conversion.

❒ Detail descriptions of register (continued)

● CCWCWAB（α motor rotation direction）

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							CCWCWAB								

● CCWCWCD（β motor rotation direction）

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							CCWCWCD								

CCWCWAB and CCWCWCD set the rotation direction of α motor and β motor respectively.

Setup value	Motor rotation direction
0	Forward
1	Reverse

● BRAKEAB（α motor brake）

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						BRAKEAB									

● BRAKECD（β motor brake）

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						BRAKECD									

BRAKEAB and BRAKECD set the brake mode of α motor and β motor respectively.

Setup value	motor brake
0	Normal operation
1	Brake mode

Both of upper-side P-ch MOSs of output H bridge turn on in brake mode. The brake mode is not used in normal operation, and is used for emergency shutdown. It is recommended to use only in abnormal state.

❒ Detail descriptions of register (continued)

● ENDISAB (α motor Enable/Disable)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					ENDISAB										

● ENDISCD (β motor Enable/Disable)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					ENDISCD										

ENDISAB and ENDISCD configure the setting for output stage control of α motor and β motor respectively.

The output becomes the state of OFF (Hi-Z) at ENDISxx = 0. However, internal excitation position counter keeps counting even ENDISxx = 0. Therefore, when stopping the motor during normal operation, set PSUMxx[7:0] = 0 (not ENDISxx = 0).

Setup value	Motor output condition
0	Output OFF (Hi-Z)
1	Output ON

● MICROAB [1:0] (α motor quasi-sin wave division number)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		MICROAB													

● MICROCD[1:0] (β motor quasi-sine wave division number)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		MICROCD													

MICROAB [1:0] and MICROCD [1:0] set the number of quasi-sine wave divisions for α motor and β motor respectively. Waveform example for 64 divisions is on page 35.

Setup value	Number of divisions
00	256
01	256
10	128
11	64

❒ Detail descriptions of register (continued)

● INTCTAB [15:0] (α motor step cycle setup)

Address			25h			Initial Value			0080h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
INTCTAB[15:0]															

● INTCTCD [15:0] (β motor step cycle setup)

Address			2Ah			Initial Value			0080h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
INTCTCD[15:0]															

INTCTAB[15:0] and INTCDCD[15:0] set the step cycle of α motor and β motor respectively. Since the step cycle is converted to 64-step inside, motor rotation speed becomes the same regardless of the number of divisions set by MICROxx[1:0].

Setting value	Step cycle		
	64-step	128-step	256-step
0	0	0	0
1	444ns	222ns	111ns
Max	29.1ms	14.6ms	7.3ms
n	12n/27MHz	6n/27MHz	3n/27MHz

If maximum duty is set to other than "0" at INTCTxx [15:0] = 0, the position is held in the state of excitation.

If a motor can hold the position by cogging torque without motor current, the position is held even if the maximum duty is set to 0.

e. g.) If ITCTAB[15:0] = 400 is set, time of 1 step for 64-step is

$$12 \times 400 / 27\ \text{MHz} = 0.178\ \text{ms}$$

Therefore, period of one sinusoidal wave cycle is 11.4 ms (87.9

Hz). This is the same for 128-step and 256-step.

❒ Detail descriptions of register (continued)

● FZTEST[4:0] (Test signal output setup)

Address			21h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
											FZTEST[4:0]				

● TESTEN1(Test setting 1)

Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								TESTEN1							

● TESTEN2(Test setting 2)

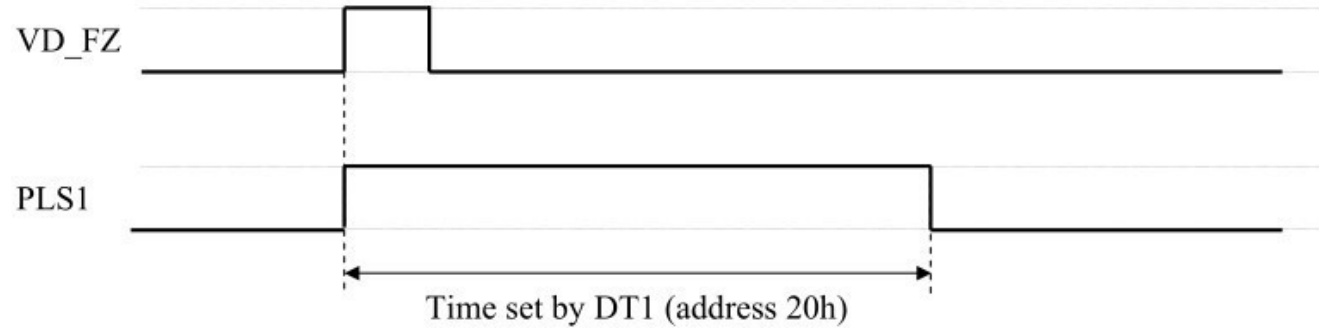
Address			21h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								TESTEN2							

FZTEST[4:0] makes a choice of the test signal which is output to PLS1 and PLS2 pins. TESTEN1 (0Bh) and TESTEN2 (21h) should be set to "1" in order to enable the test signal. Since the test signal used in our company is output, do not set other than the setups described in the following table.

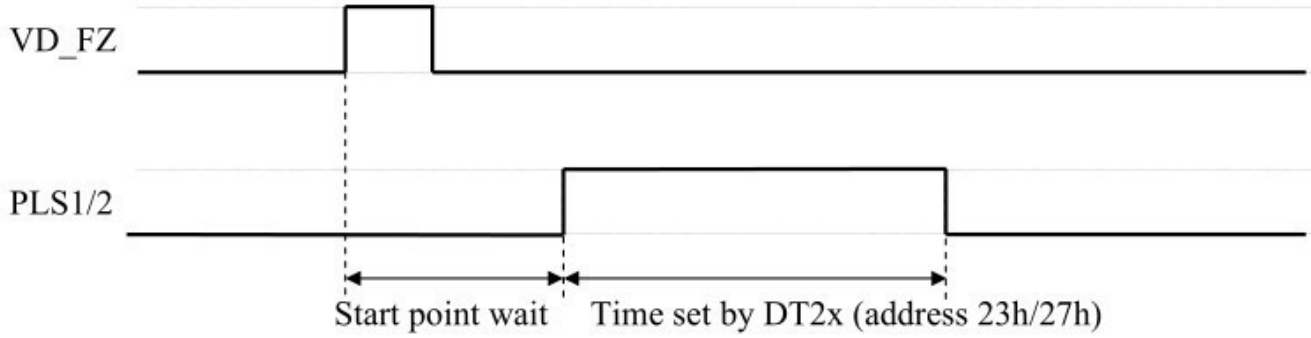
Setup value	Step cycle		Description
	PLS1	PLS2	
0	PLS1	PLS2	Pulse 1/2 normal function
1	Start point wait	0	"H" output during start point wait
2	Start point excitation wait A	Start point excitation wait B	"H" output during start point excitation wait
3	ENDISAB	ENDISCD	ENDISxx setting
4	CCWCWAB	CCWCWCD	CCWCWxx setting
5	Pulse output monitor A	Pulse output monitor B	During motor rotation, "H"/"L" changes at the speed of 64-step
6	PWM cycle monitor	0	PWM frequency signal for micro step
7	Pulse completion output A	Pulse completion output B	"H" output during motor rotation

❒ Detail descriptions of register (continued)

Waveform for each test signal is described below.



Start point excitation wait

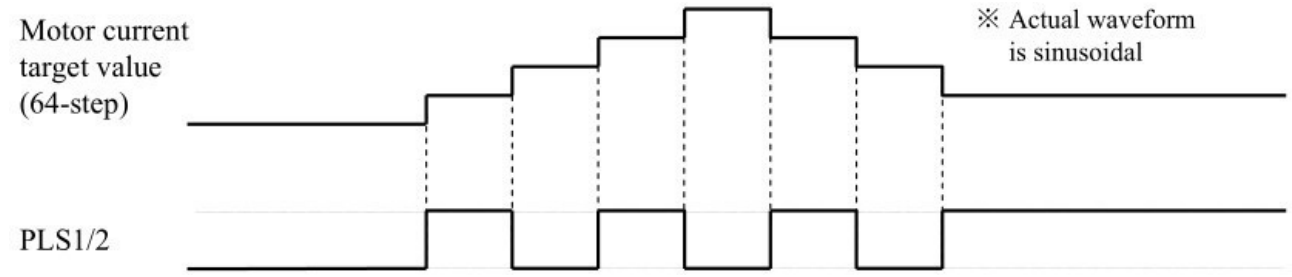


ENDISxx

CCWCWxx

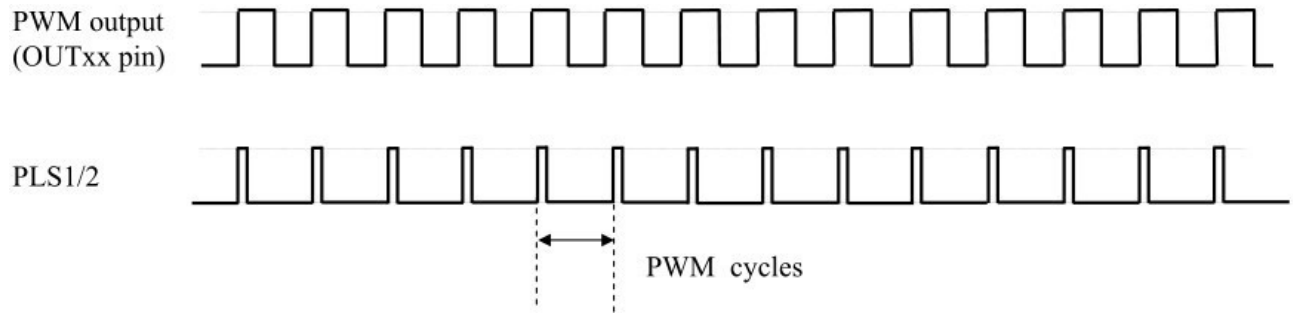
❒ Detail descriptions of register (continued)

Pulse output monitor

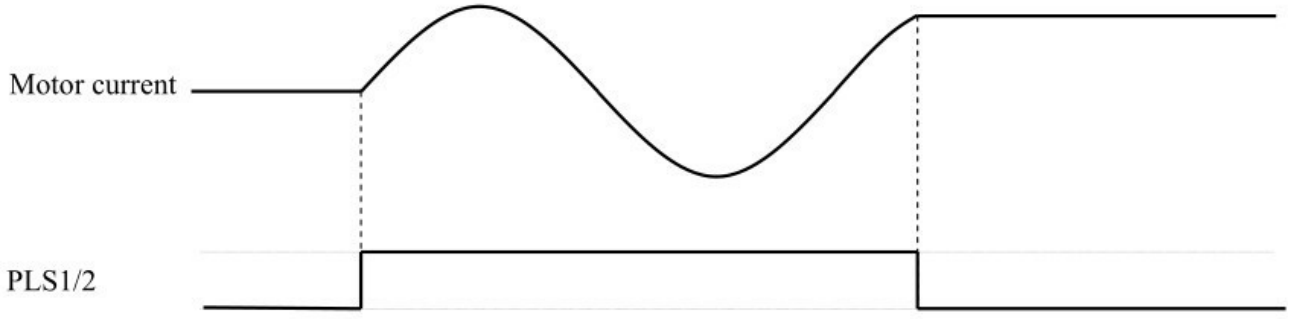


For 128-step and 256-step, “H”/“L” of PLS1/2 changes every 2 and 4 steps respectively.

PWM cycle monitor



Pulse completion output



❒ PWM frequency setup and Maximum duty setup

The setups method example of PWM frequency and maximum duty are shown as follows.

PWM frequency setup

PWM frequency is calculated by the following formula with PWMMODE [4:0] and PWMRES[1:0] .

PWM frequency = OSC frequency / ((PWMMODE×2 3) × 2 PWMRES)

PWM frequency corresponding to each setup value of PWMMODE and PWMRES.

Note that there may be two kinds of combination of the setup value corresponding to PWM frequency. For example, there are two kinds of setup to realize that PWM frequency is 56.3 kHz.

PWMMODE = 30，PWMRES = 1 PWMMODE = 15，PWMRES = 2

In such a case, PWMMODE should be set so that it is a larger value as described here in below.

Maximum duty setup

PWM output maximum duty is calculated by the following formula.

Maximum duty = PPWx / (PWMMODE × 8)

For example, when PWM frequency is set as follows,

PWMMODE = 30，PWMRES = 1 → PWM frequency = 56.3 kHz maximum duty becomes the following value by setting to PPWx = 200.

200 / (30 × 8) = 0.83

Since resolution of sine wave amplitude is determined by PPW setup, PWMMODE should be also set to as large a value as possible so that PPW becomes as large as possible.

❒ Peak duty setup which exceeds 100%

PWM maximum duty at peak position of micro step current is determined by PWMMODE[4:0] and PPWx[7:0].

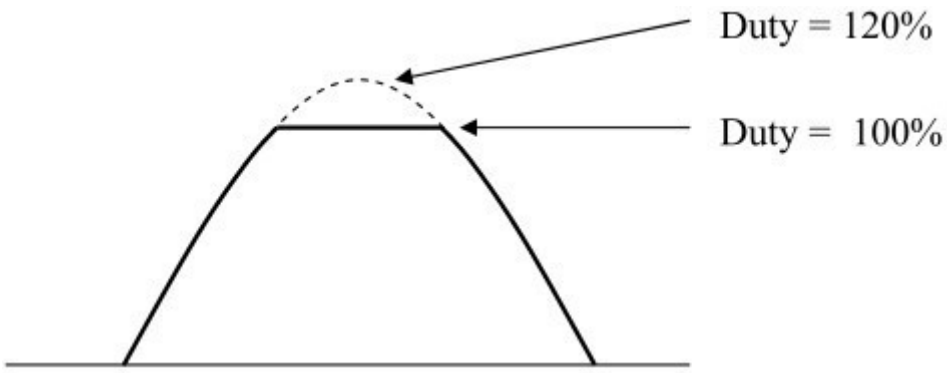
Maximum duty = PPWx / (PWMMODE × 8)

Maximum duty may exceed 100% depending on the setup values of PWMMODE and PPWx.

Since the duty does not certainly exceed 100% at PWM operation in this case, the peak point of sine wave (current waveform) becomes flat as follows.

Example 1) When PWMMODE = 10, PPWx = 96,

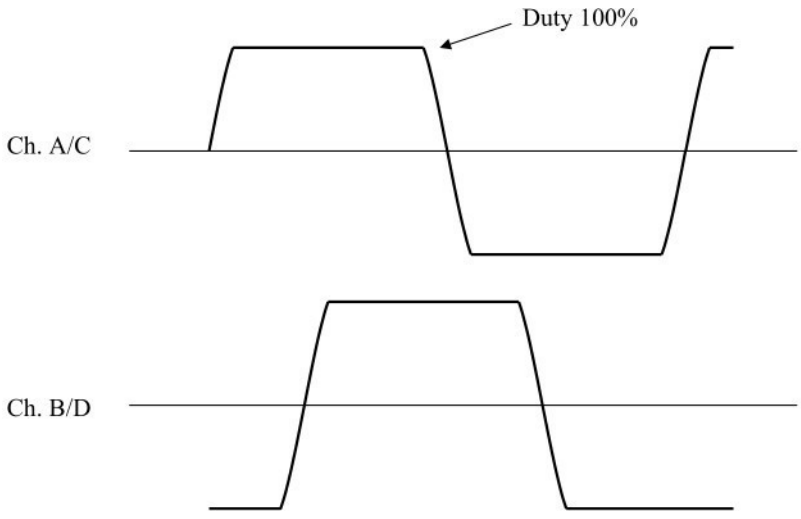
Maximum duty = 96 / (10 × 8) = 120% The target current waveform is indicated as the following full line.



Example 2) When PWMMODE = 5, PPWx = 255,

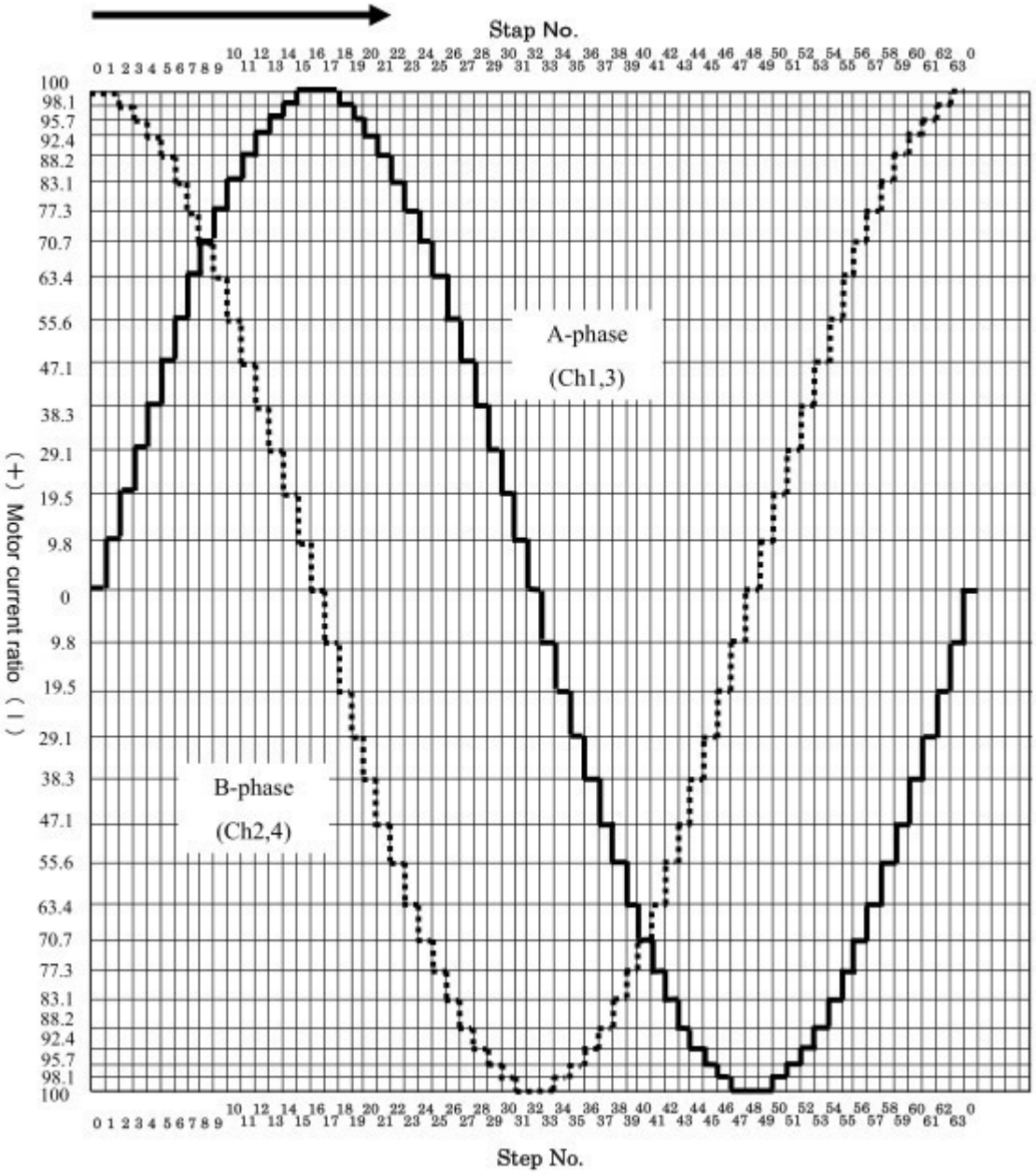
Maximum duty = 255 / (5 × 8) = 638%

The target current waveform becomes close to 2-phase drive.



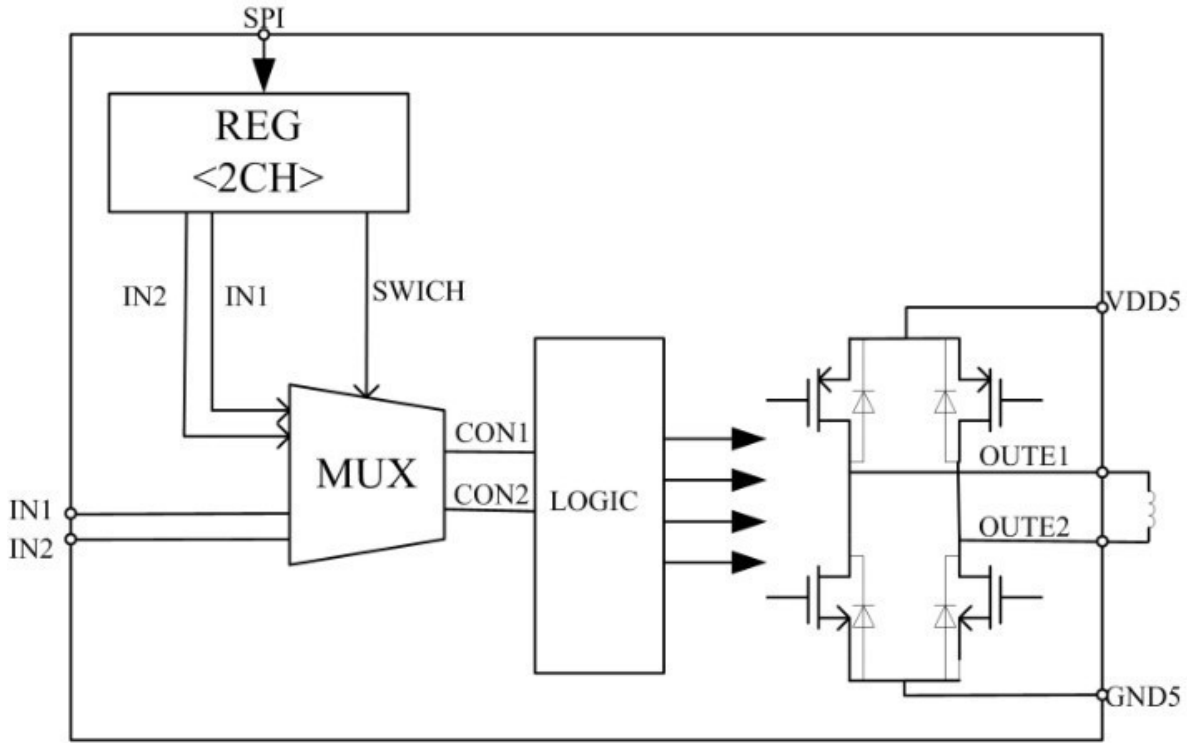
12. Micro step drive (64-step)

（1）Forward rotation



13. DC Motor Driver

❒ Block Diagram



❒ This block is a DC motor driver for IR-CUT, it is driven by PWM control mode.

❒ there are two input control modes: direct external input control mode and SPI internal input control mode.

❒ Electrical Characteristics at VDD5, MVCCx = 5.0 V, DVDD = 3.3 V, RL=20Ω， Ta=25℃

Notes) Ta = 25°C±2°C unless otherwise specified.

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
Motor driver 2 (ir-cut) VDD5 = 5 V, RL = 20 Ω, TA = 25°C, unless otherwise noted						
Roncut	Roncut	Roncut	Roncut	Roncut	Roncut	Ω
Ileakcut	Ileakcut	Ileakcut	Ileakcut	Ileakcut	Ileakcut	μA
t1	Output enable time				300	ns
t2	Output disable time				300	ns
t3	Delay time, INx high to OUTx high				160	ns
t4	Delay time, INx low to OUTx low				160	ns
t5	Rise time		30		188	ns
t6	Fall time		30		188	ns

td	Delay time from SPI in to OUTE on			25* TSCK		s

❒ Detail descriptions of register

DC Motor can be controlled station by the following registers.

● INSWICH (input mode select)

Address			2Ch			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
													INSWICH		

Setup value	state of the control	PMW	Control of the driver
0	external control (initial setting)	IN1、IN2 control	IN1、IN2 control
1	internal control	resistor control	resistor control

● IN1 (internal input control one)

Address			2Ch			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
														IN1	

● IN2 (internal input control one)

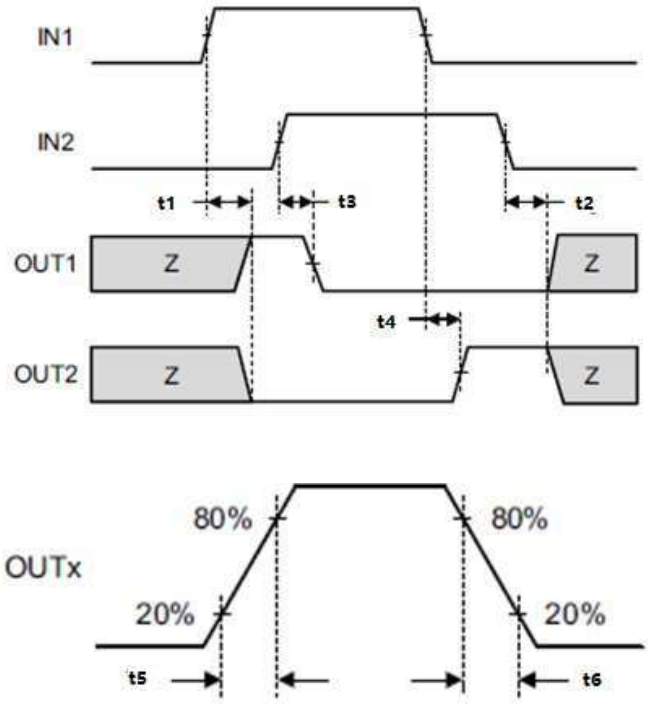
Address			2Ch			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
															IN2

IN1 and IN2 set the output station of the motor respectively.

Setup value		output		Motor station
IN1	IN2	OUT1	OUT2	
0	0	Z	Z	Coast
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake

❒ Detail timing requirements by the direct external input control mode

The delay time of the input to the output all less than 300ns.



❒ Detail timing requirements by the SPI input control mode

Because SPI serial input writes registers (22 data and there are 3 control bits are written at a time,), so the transmission delay time from writing register 2CH to the control time work is about Tsclk*25.

If the serial clock for writing data is 0.5MHz, Then the digital delay time is 25*1/0.5M=50us, at which time the maximum output frequency of H-bridge is 10KHz.

14. LED Driver

❒ Electrical Characteristics at VDD5, MVCCx = 5.0 V, DVDD = 3.3 V

Notes) Ta = 25°C±2°C unless otherwise specified.

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
LED driver						
RonLED	Output ON resistance	I=20mA, 5V cell		2.5		Ω
IleakIR	Output leak current				0.8	μA

❒ Detail descriptions of register

LED can be controlled ON/OFF by the following registers.

● LEDA (LED A setup)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				LEDA											

● LEDB (LED B setup)

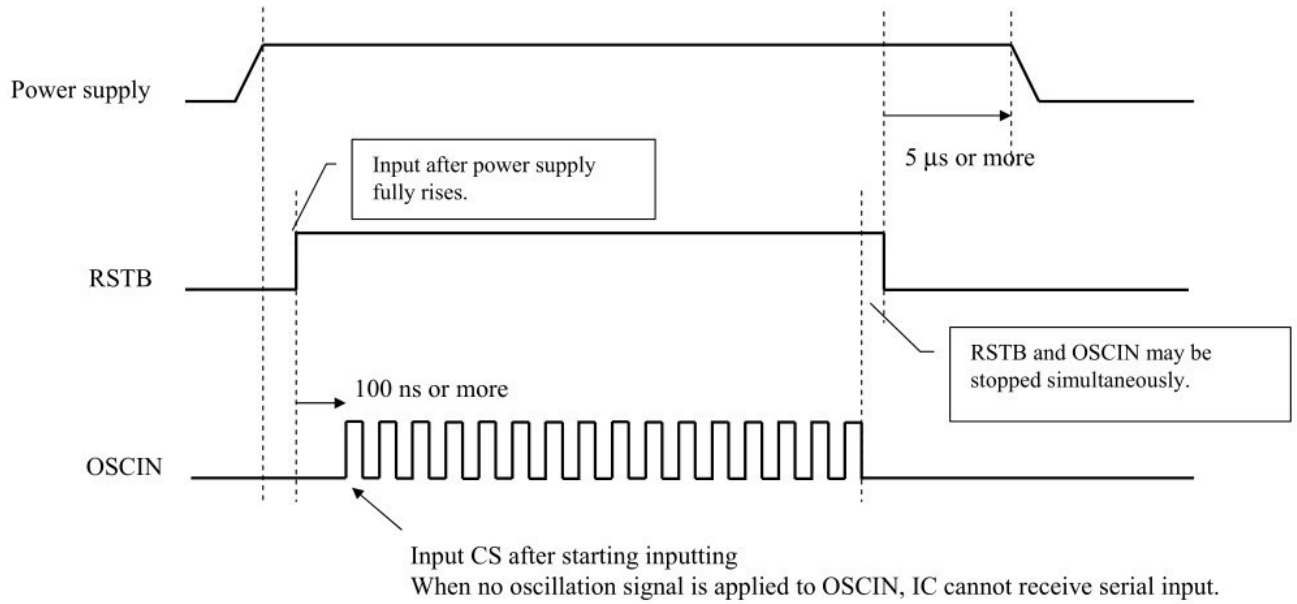
Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				LEDB											

LEDA and LEDB set the output of LED A and LED B respectively.

Setup value	LED output
0	OFF
1	ON

1. Start / Stop sequence

The Start / Stop sequence of power supply, RSTB, and OSCIN is shown as follows.



2. Input capacitance of input pin

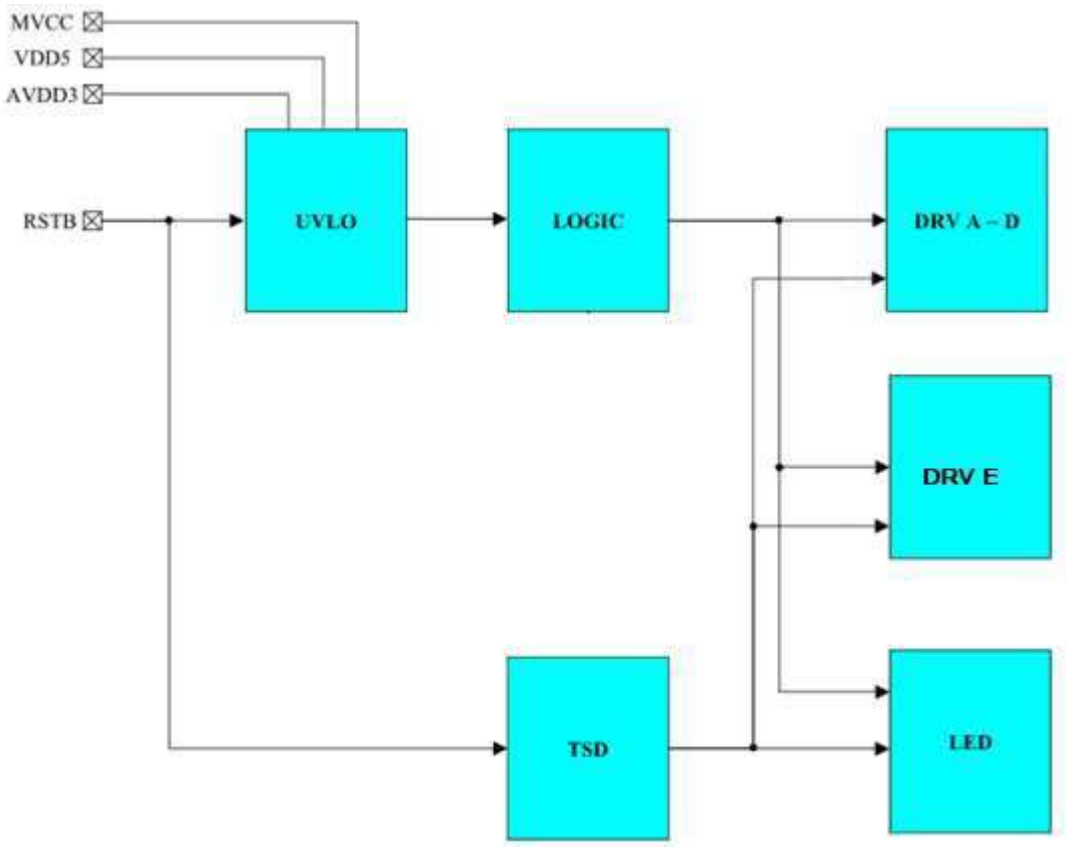
Input capacitance of input pin is 10 pF or less.

3. Timing of OSCIN and VD signal

Since the processing which VD signal (VD_FZ input) is synchronized with OSCIN is performed in this IC, OSCIN and VD signal do not have restrictions of input timing.

Reset / Protection circuit

❒ Block Diagram / Specifications



Stop direction (Enable → Disable) is shown as above. The specifications are shown as follows.

	COMMON	FZ output	IR-CUT output	LED
RSTB pin	Disable	Logic reset → Output OFF		
Thermal shutdown (TSD)	X	Output OFF		
Under-voltagelock-out (UVLO)	X	Logic reset → Output OFF		

※Note 1 ×: Don't care

※Note 2 The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.

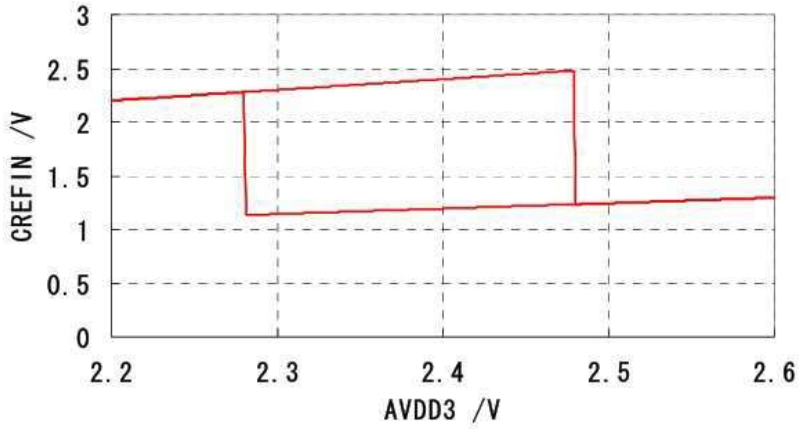
❒ Electrical Characteristics (Reference values for design) at VDD5, MVCCx = 5.0 V, DVDD= 3.3 V

Notes) Ta = 25°C±2°C unless otherwise specified.

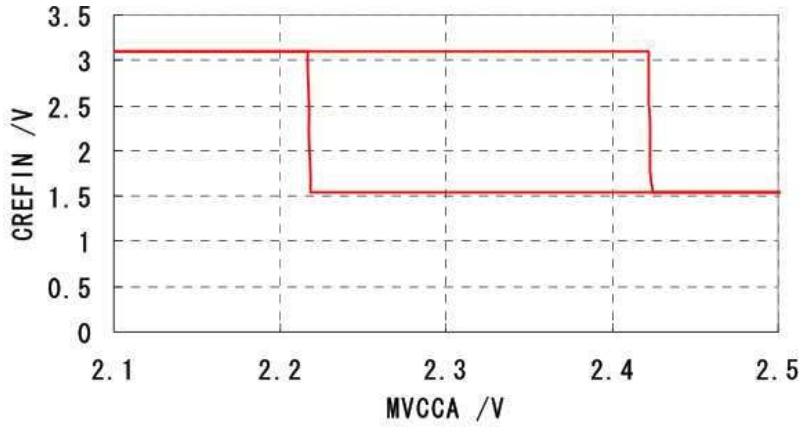
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection. If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

Symbol	Parameter	Condition	Limits			Unit	Note
			Min	Typ	Max		
Thermal Shutdown							
Ttsd	Thermal shutdown operation temperature	Die temperature TJ		150		℃	*1
ΔTTSD	Thermal shutdown hysteresis width			40		℃	*1
Supply voltage monitor circuit							
Vrston	3.3 V Reset operation			2.7		V	*1
Vrsthys	3.3 V Reset hysteresis			0.15		V	*1
VrstFZon	MVCCx Reset operation			2.5		V	*1
VrstFZhys	MVCCx Reset hysteresis			0.10		V	*1
VrstlSon	VDD5 Reset operation			2.5		V	*1
VrstlShys	VDD5 Reset hysteresis			0.1		V	*1
Digital input							
Vin(H)	High-level input voltage			1.36		V	
Vin(L)	Low-level input voltage			1.02		V	
Vhysin	Input hysteresis width			0.34		V	
Rpullret	Input pull-down resistance	RSTB		100		KΩ	

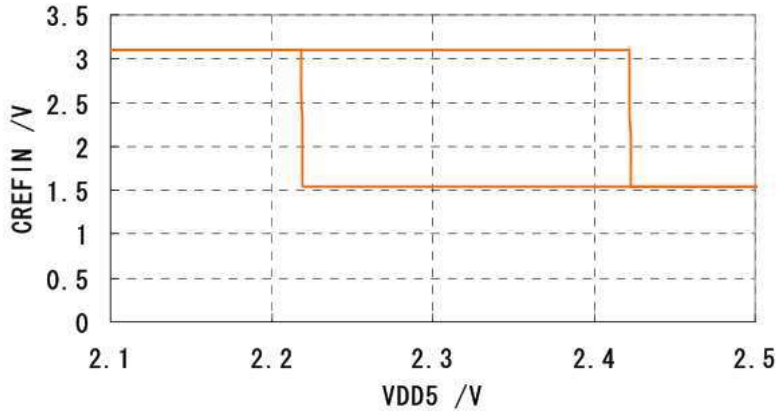
Characteristic of supply voltage monitor.



(1) AVDD3
Operation voltage : 2.28V
Return voltage : 2.48V



(2) MVCC
Operation voltage : 2.22V
Return voltage : 2.42V



(3) VDD5
Operation voltage : 2.22V
Return voltage : 2.42V

15. Application schematic

The Power supply of MVCCA, MVCCB and VDD5 should be will filtered by Bulk Capacitor and Bypass Capacitor for each Power in. The recommended value is 10uF //0.1uF.

15.1 Application with crystal as below, the frequence should be 5 - 27MHz.

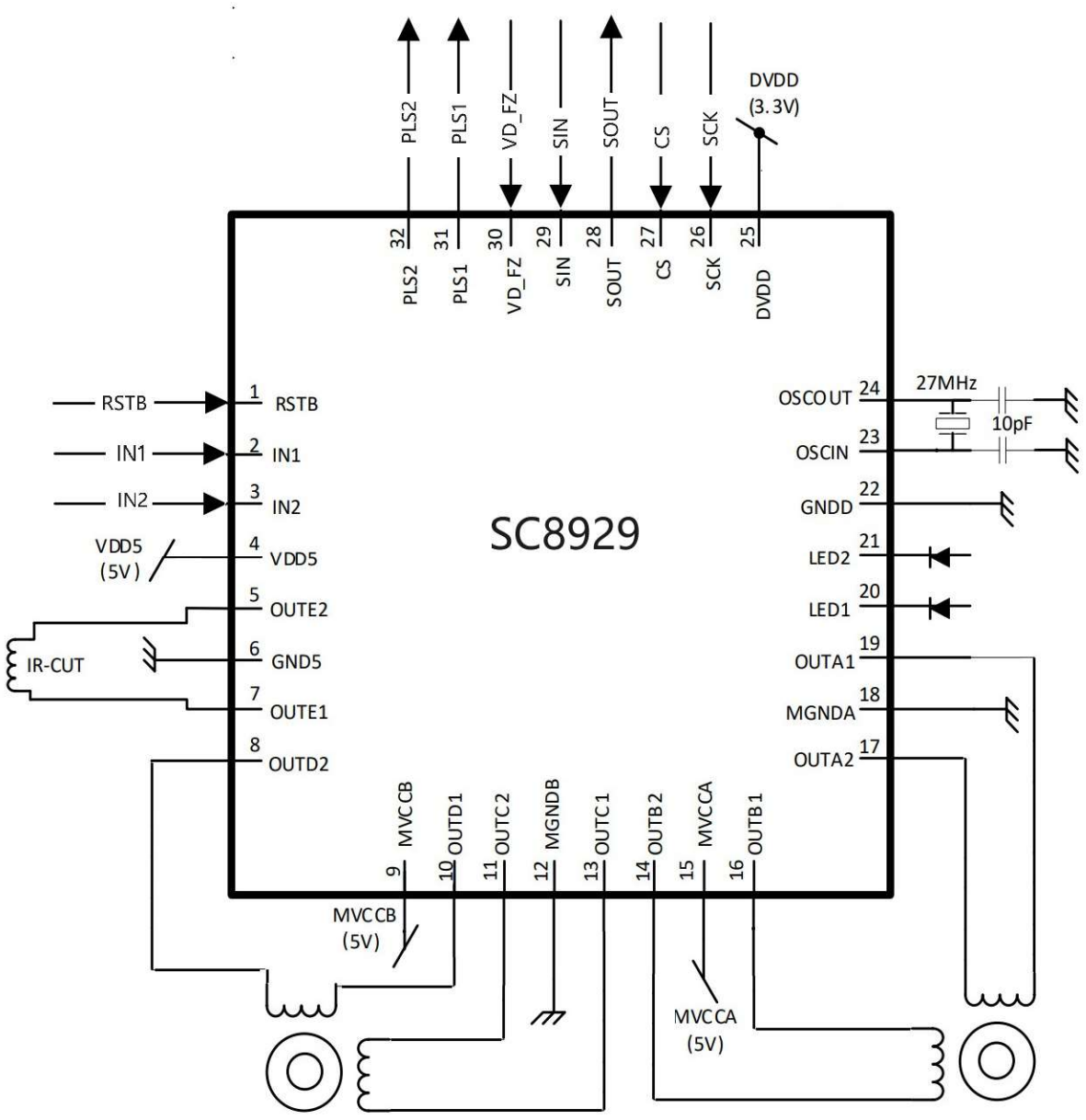


Fig 15.1 Application schematic with Crystal

15.2 Application schematic with External clock

The clock should be minimum 1.3V for AC Coupling (through 0.1uF); or 2.4V for DC Coupling.

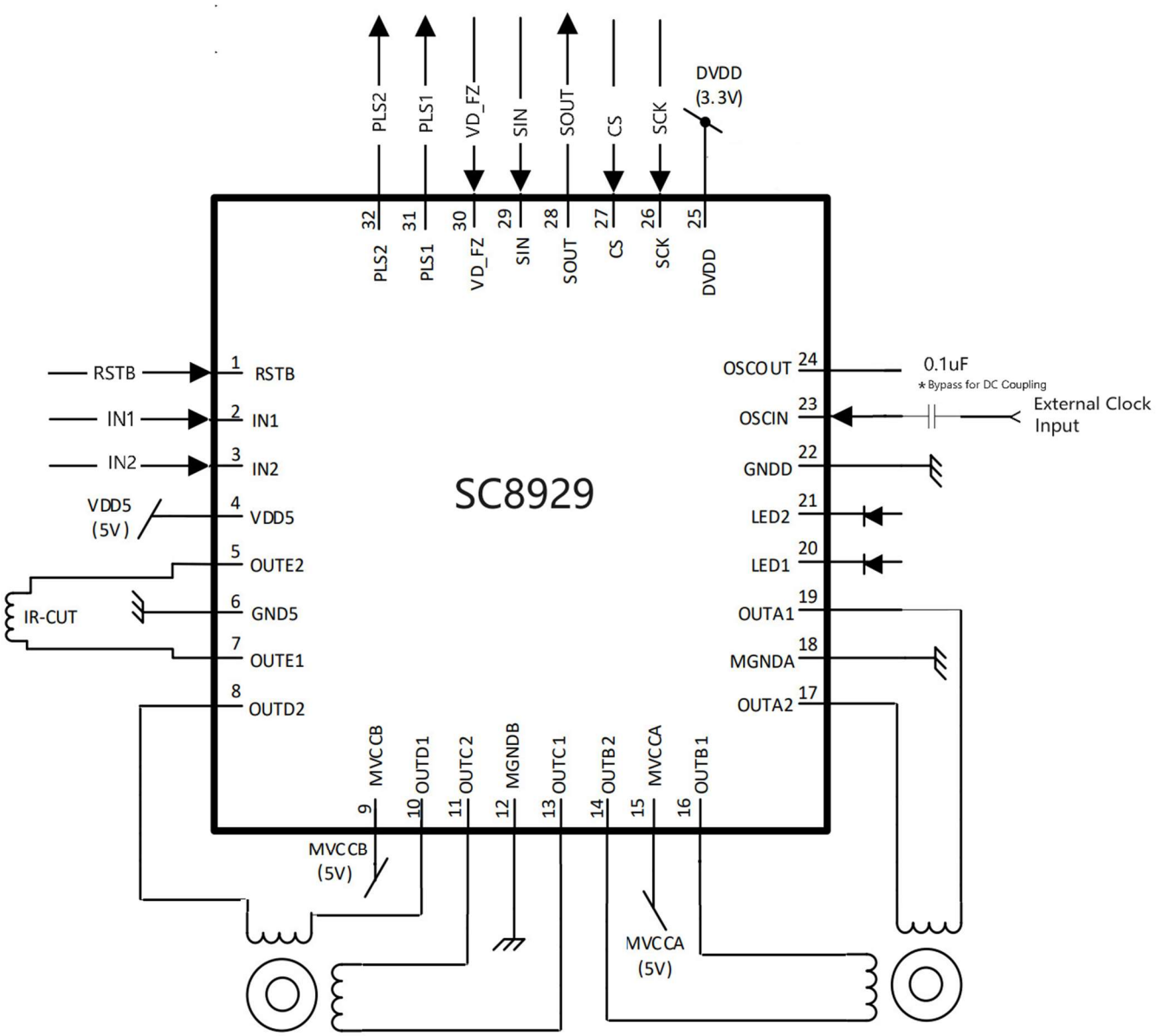
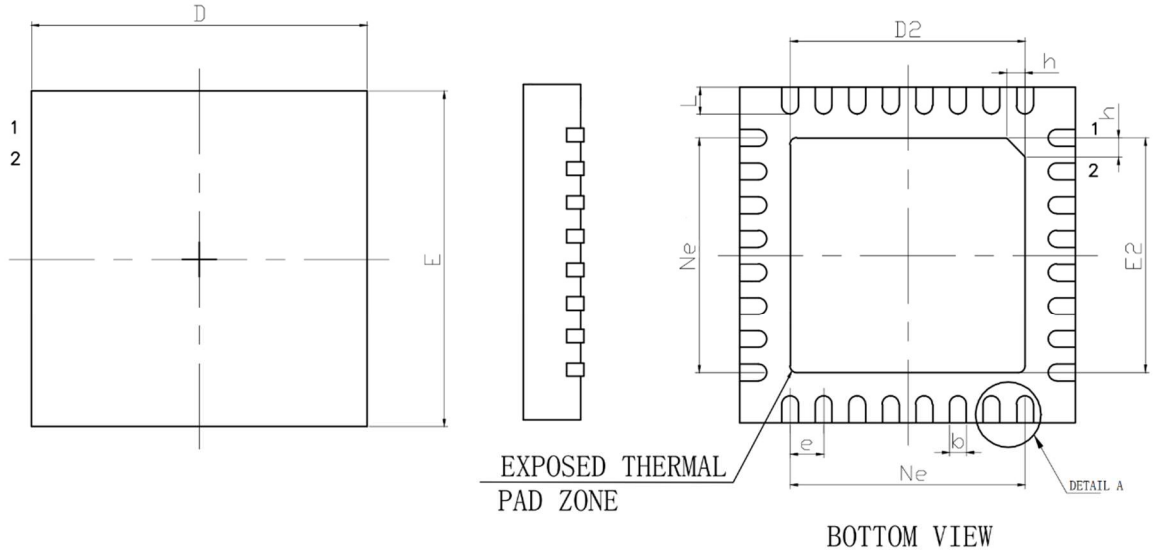
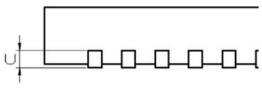


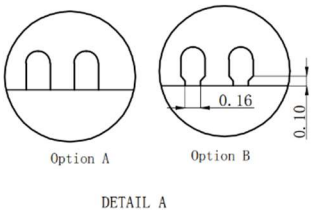
Fig 15.2 Application schematic with external Clock

16. Package

QFN44 0505X0.75-0.35







SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
	0.85	0.90	0.95
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸	150x150		130x130

USAGE NOTES

1. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
2. Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such
3. as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.
4. Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.
5. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit- board), it might smoke or ignite.
6. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
7. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
8. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short)
9. And, safety measures such as an installation of fuses are recommended because the extent of the above- mentioned damage and smoke emission will depend on the current capability of the power supply.
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
11. Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.
12. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
13. The product which has specified ASO (Area of Safe Operation) should be operated in ASO
14. Verify the risks which might be caused by the malfunctions of external components.
15. Take time to check the characteristics on use. When changing an external circuit constant for use, consider not only static characteristics, but also transient characteristics and external parts with respect to the characteristics difference among ICs so that you can get enough margin. Moreover, consider the influence of electric charge remaining in an external capacitor on rising/falling of power supply.
16. Apply voltage from a low-impedance to power supply pins and connect a bypass capacitor to the LSI as near as possible.