SC7125
High Speed
Triple 8-Bit Video D/A Converter

FEATURES

- 240 MSPS THROUGHPUT RATE
- TRIPLE 8-bit D/A CONVERTER
- WIDE SPURIOUS-FREE DYNAMIC RANGE:
  69 dB at f_{CLK} = 50 MHz; f_{OUT} = 1 MHz
  70dB at f_{CLK} = 100 MHz; f_{OUT} = 2.01 MHz
- DIFFERENTIAL CURRENT OUTPUT
- RS-343A-/RS-170-COMPATIBLE OUTPUT
- SINGLE 5/3.3V POWER SUPPLY
- TTL-COMPATIBLE INPUTS
- OUTPUT CURRENT RANGE: 2.0 mA TO 26.5 mA
- LOW POWER STANDBY MODE (1mW)
- 48-PIN LQFP PB-FREE PACKAGE

APPLICATIONS

- IMAGE PROCESSING
- HIGH RESOLUTION COLOR GRAPHICS
- VIDEO SIGNAL RECONSTRUCTION
- INSTRUMENTATION

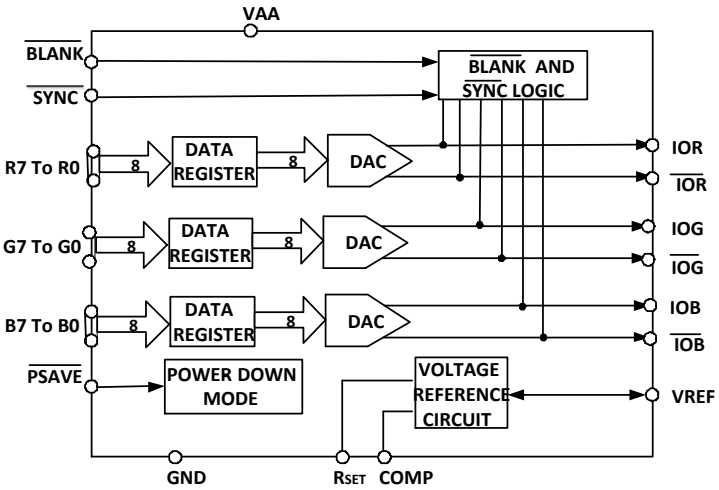
DESCRIPTION

The SC7125 is a low cost general-purpose triple high-speed D/A converter, which is optimized for video graphics applications. The SC7125 contains three matched 8-bit DACs, which adopt an advanced, high speed, segmented architecture. It consists of a standard TTL input interface, a set of high impedance, analog output current sources and a complementary output. The SC7125 has additional video control signals, composite $\overline{SYNC}$ and $\overline{BLANK}$. The SC7125 also has a power save mode. Its monolithic CMOS construction ensures greater functionality. Featured by a proprietary switching technique and segmented current source architecture, the SC7125 dramatically reduce spurious components and enhance dynamic performance. Through the Edge-triggered input latches and a built-in 1.235V temperature compensated bandgap reference, the SC7125 provide the costumers an easy and cost-saving choice.
The SC7125 is developed for low-power low-voltage applications, whose supply range is from +2.7V to +5V. The SC7125 is specified over the industrial (–40°C to +85°C) or commercial (0°C to +70°C) temperature ranges.

PRODUCT HIGHLIGHTS

- 240MHz MAXIMUM SAMPLING CLOCK FREQUENCY
- 8BIT RESOLUTION
- ON-CHIP 1.235V REFERENCE
- ADJUSTABLE SCALE FROM 2mA TO 26.5mA
- HIGH ESD CAPABILITY (>8000V HBM)

FUNCTIONAL BLOCK DIAGRAM



REV. 1.1.0

SPECIFICATIONS

5 V SPECIFICATIONS

(V_{AA} = 5.0 V±5%, R_{SET} = 560 Ω, Typical values are at T_A = +25°C, unless otherwise noted.)

Table 1.

PARAMETER	MIN	TYP	MAX	UNITS
RESOLUTION(Each DAC)		8		Bits
MONOTONICITY			Guaranteed	Monotonic
DC ACCURACY				
Differential Nonlinearity (DNL)	-1	±0.25	+1	LSB
Integral Nonlinearity (INL)	-1	±0.25	+1	LSB
DIGITAL INPUT				
Input High Voltage, V_{IH}	2			V
Input Low Voltage, V_{IL}		0.8		V
Input Capacitance, C_{IN}		10		pF
ANALOG OUTPUT				
Offset Error	–0.13		+0.13	% of FSR
Gain Error (With Internal Reference)	–5	±1	+5	% of FSR
Full-Scale Output Current (1)	2.0		26.5	mA
(2)	2.0		18.5	mA
DAC-to-DAC Matching		1	3	%
Output Resistance		100		kΩ
Output Capacitance		5		pF
VOLTAGE REFERENCE, EXTERNAL AND INTERNAL				
Reference Voltage	1.12	1.235	1.35	**V**
POWER SUPPLY				
Analog Supply Current		62	68	mA
Digital Supply Current (3)		3	7	mA
Standby Supply Current		0.2		mA
Power Supply Rejection Ratio	–0.5		+0.5	% of FSR**/V**

NOTES

(1) Green DAC, $\overline{SYNC}$ tie to logic 1.

(2) RGB DAC, $\overline{SYNC}$ tie to logic 0.

(3) Fclk=50MHz

3.3V SPECIFICATIONS

(V_{AA} = 3.3 V±10%, R_{SET} = 560 Ω, Typical values are at T_A = +25°C, unless otherwise noted.)

Table 2.

PARAMETER	MIN	TYP	MAX	UNITS
RESOLUTION(Each DAC)		8		Bits
MONOTONICITY			Guaranteed Monotonic	
DC ACCURACY				
Differential Nonlinearity (DNL)	-1	±0.2	+1	LSB
Integral Nonlinearity (INL)	-1	±0.2	+1	LSB
DIGITAL INPUT				
Input High Voltage, V_{IH}	2			V
Input Low Voltage, V_{IL}		0.8		V
Input Capacitance, C_{IN}		10		pF
ANALOG OUTPUT				
Offset Error	–0.13		+0.13	% of FSR
Gain Error (With Internal Reference)	–5	±1	+5	% of FSR
Full-Scale Output Current (1)	2.0		26.5	mA
(2)	2.0		18.5	mA
DAC-to-DAC Matching		1	3	%
Output Resistance		100		kΩ
Output Capacitance		5		pF
VOLTAGE REFERENCE, EXTERNAL AND INTERNAL				
Reference Voltage	1.12	1.235	1.35	V
POWER SUPPLY				
Analog Supply Current		62	68	mA
Digital Supply Current (3)		3	7	mA
Standby Supply Current		0.2		mA
Power Supply Rejection Ratio	–0.5		+0.5	% of FSR/V

NOTES

(1) Green DAC, $\overline{SYNC}$ tie to logic 1.

(2) RGB DAC, $\overline{SYNC}$ tie to logic 0.

(3) Fclk=50MHz

5 V TIMING SPECIFICATIONS

(V_{AA} = 5.0 V±5%, R_{SET} = 560 Ω, Typical values are at T_A = +25°C, unless otherwise noted.)

Table 4.

PARAMETER	Symbol	MIN	TYP	MAX	UNITS	Conditions
ANALOG OUTPUTS						
Analog Output Delay	t1		4.0		ns	
Analog Output Rise/Fall Time	t2		1.0		ns	
Analog Output Transition Time	t3		15		ns	
CLOCK CONTROL						
Data and Control Setup	ts	1.5			ns	
Data and Control Hold	th	2.5			ns	
CLOCK Period	tp	4.2			ns	
CLOCK Pulse Width High	t_H	4			ns	f_{CLK} = 100 MHz
CLOCK Pulse Width Low	t_L	4			ns	f_{CLK} = 100 MHz

3.3 V TIMING SPECIFICATIONS

(V_{AA} = 3.3 V±10%, R_{SET} = 560 Ω, Typical values are at T_A = +25°C, unless otherwise noted.)

Table 6.

PARAMETER	Symbol	MIN	TYP	MAX	UNITS	Conditions
ANALOG OUTPUTS						
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Analog Output Rise/Fall Time	t2		1.0		ns	
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Data and Control Setup	ts	1.5			ns	
Data and Control Hold	th	2			ns	
CLOCK Period	tp	4.2			ns	
CLOCK Pulse Width High	t_H	4			ns	f_{CLK} = 100 MHz
CLOCK Pulse Width Low	t_L	4			ns	f_{CLK} = 100 MHz

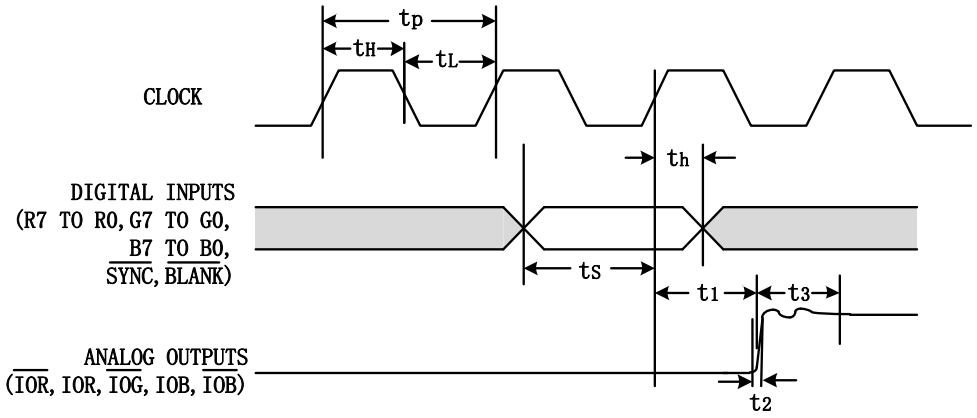


Figure 2. Timing Diagram

PIN CONFIGURATION

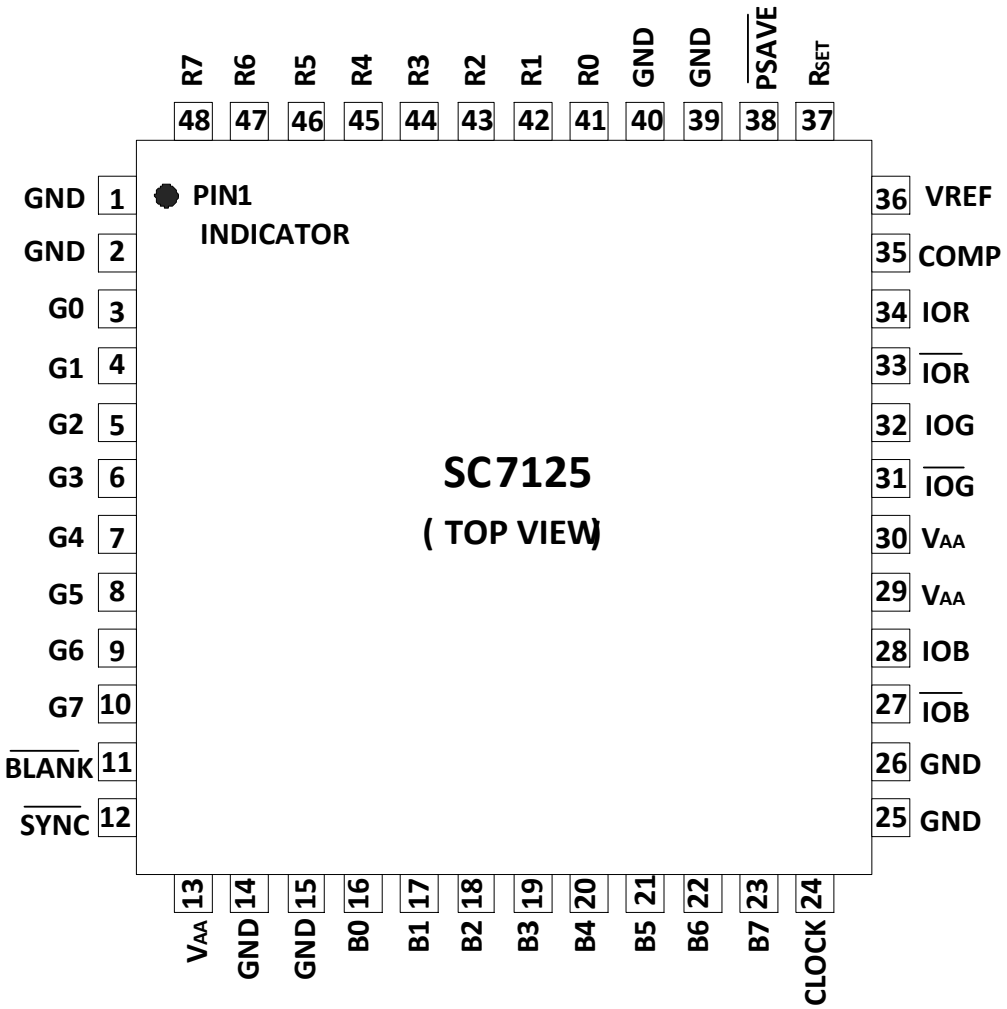


Figure3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Name	Function
3-10	**G0-G7**	Green Channel Data Inputs (TTL Compatible).Data is registered on the rising edge of CLOCK. G7 is the Most Significant Data Bit. Unused inputs should be connected to GND.
11	**$\overline{\text{BLANK}}$**	Blanking Control Input (TTL Compatible). A Logic 0 on this control input drives the analog outputs, IOR, IOB, and IOG, to the reference blanking level. The rising edge of CLOCK latches the $\overline{\text{BLANK}}$ signal. When $\overline{\text{BLANK}}$ is a Logic 0, the value of R0 to R9, G0 to G9, and B0 to B9 are ignored.
12	**$\overline{\text{SYNC}}$**	Composite Sync Control Input (TTL Compatible). A Logic 1 on the $\overline{\text{SYNC}}$ input switches on a 40 IRE current source, which is internally connected to the IOG analog output. $\overline{\text{SYNC}}$ should only be asserted during the blanking interval since it does not override any other control or data input. The rising edge of CLOCK latches the $\overline{\text{SYNC}}$ signal. The $\overline{\text{SYNC}}$ should be asserted to Logic 0 if sync information is not required on the green channel.
13,29,30	**V_{AA}**	Power Supply. All V_{AA} Pins must be connected.
16-23	**B0-B7**	Blue Channel Data Inputs (TTL Compatible).Data is registered on the rising edge of CLOCK. B7 is the Most Significant Data Bit. Unused inputs should be connected to GND.
24	**CLOCK**	Clock Input (TTL Compatible). Data and control signals are registered on positive edge of clock.
1-2,14-15,39-40,25-26	**GND**	Ground. ALL GND pins must be connected.
27	**$\overline{\text{IOB}}$**	Complementary Blue Channel Current Output. Full-scale current when B0-B9 are 0s. When it is not required, it should be tied to ground.
28	**IOB**	Blue Channel Current Output. It is capable of directly driving a doubly terminated 75 Ω coaxial cable. The Full-scale current output will be shown on this pin when B0-B9 are 1s.
31	**$\overline{\text{IOG}}$**	Complementary Green Channel Current Output. Full-scale current when G0-G9 are 0s. When it is not required, it should be tied to ground.
32	**IOG**	Green Channel Current Output. It is capable of directly driving a doubly terminated 75 Ω coaxial cable. The Full-scale current output will be shown on this pin when G0-G9 are 1s.
33	**$\overline{\text{IOR}}$**	Complementary Red Channel Current Output. Full-scale current when R0-R9 are 0s. When it is not required, it should be tied to ground.
34	**IOR**	Red Channel Current Output. It is capable of directly driving a doubly terminated 75 Ω coaxial cable. The Full-scale current output will be shown on this pin when R0-R9 are 1s.
35	**COMP**	Bandwidth/Noise Reduction Node. Add 0.1μF to V_{AA} for optimum performance.
36	**VREF**	Reference Voltage Input/Output (1.235V).
37	**R_{SET}**	The full-scale current driving on each of the output channels is determined by the resistor (R_{SET}) connected between this pin and GND. For nominal video levels into a doubly terminated 75 Ω load, R_{SET} equals to 530 Ω. The relationship between R_{SET} and the full-scale output current on IOR, IOG($\overline{\text{SYNC}}$ tied Logic 0), and IOB is given by: IOR, IOB, IOG (mA) = 7989.6 × VREF (V)/ R_{SET} (Ω) The relationship between R_{SET} and the full-scale output current on IOG ($\overline{\text{SYNC}}$ being asserted to Logic 1) is given by: IOG (mA) = 11,445 × VREF (V)/ R_{SET} (Ω)
38	**$\overline{\text{PSAVE}}$**	Power-Save Control Input (Active Low). A built-in pull-up circuit is attached.
41-48	**R0-R7**	Red Channel Data Inputs (TTL Compatible).Data is registered on the rising edge of CLOCK. R7 is the Most Significant Data Bit. Unused inputs should be connected to GND.

ORDERING GUIDE

Model	Temperature Range	Package Descriptions
SC7125AEG	-40°C to +85°C	48-Lead LQFP

DEFINITIONS OF SPECIFICATIONS

Linearity Error (Integral Nonlinearity or INL)

Linearity error is as the measure of the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)

DNL is defined as the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity

As the digital input increases, if the output will never decreases, A D/A converter is monotonic.

Gain Error

The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Offset Error

Offset Error is the measure of deviation of the output current from the ideal of zero when the inputs of D/A are all 0s.

Output Compliance Range

The maximum allowable voltage range measured at the D/A's output. Nonlinear performance might occur when the output voltage is beyond this limit.

Power Supply Rejection

Power Supply Rejection indicates the influence of variation of Power supply to the output. It is the ratio of the output change in the full-scale to the Power Supply change.

Settling Time

The time required for the output from the start of the output transition to reach and remain within a specified error band about its final value.

Glitch Impulse

Glitch Impulse is specified as the net area of the glitch in pV-s.

Blanking Level

The level separating the $\overline{\text{SYNC}}$ portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level that shuts off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)

This refers to the technique of combining the three primary colors of red, green, and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

Sync Signal ($\overline{\text{SYNC}}$)

The position of the composite video signal that synchronizes the scanning process.

Gray Scale

The discrete levels of video signal between reference black and reference white levels. A 8-bit DAC contains 1024 different levels.

Reference Black Level

The maximum negative polarity amplitude of the video signal.

Reference White Level

The maximum positive polarity amplitude of the video signal.

Sync Level

The peak level of the $\overline{\text{SYNC}}$ signal.

Video Signal

The portion of the composite video signal that varies in gray scale levels between reference white and reference black. Also referred to as the picture signal, this is the portion that can be visually observed.

Spurious-Free Dynamic Range

SFDR is defined as the ratio in dB of the RMS value of the maximum signal component to the RMS value of the next largest noise or harmonic distortion component.

Total Harmonic Distortion

THD is the ratio in dB of the RMS sum of the first six harmonic components to the RMS value of the measured input signal.

FUNCTIONAL DESCRIPTION

Figure 1 shows a block diagram of the device SC7125. The SC7125 is a fast well-matched triple DAC with current outputs optimized for graphics and video applications. Because all this circuitry is on one monolithic device, matching between the three DACs is optimized. As well as matching, the use of identical current sources in a monolithic design guarantees monotonicity and low glitch. The DAC output stages are designed to provide direct drive of doubly-terminated 75-Ω loads (37.5 Ω). The full-scale output current of all three DACs is determined by a single resistor connecting the R_{SET} pin to GND. A 530Ω resistor is suitable for most applications requiring 700-mV output levels. The on-board operational amplifier stabilizes the full-scale output current against temperature and power supply variations. The SC7125 is capable of operating up to a 240MHz sampling rate.

DIGITAL INPUTS

There are 24 bits of pixel data (color information), R0 to R7, G0 to G7, and B0 to B7, registered into the device on the rising edge of each clock cycle. These data are presented to the three 8-bit DACs and converted to three analog (RGB) output waveforms (see Figure 12).

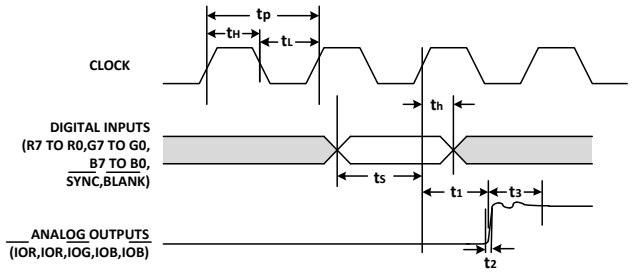


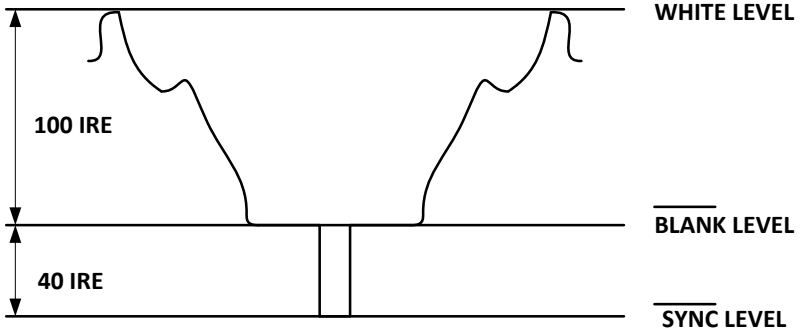
Figure12. Video Data Input/Output

The SC7125 has two additional control signals $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ which are registered on the rising edge of CLOCK to maintain synchronization with the pixel data stream. The $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ functions allow for the encoding of these video synchronization signals onto the RGB video output. This is done by adding appropriately weighted current sources to the analog outputs, as determined by the logic levels on the $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ digital inputs. Figure 13 shows the analog output, RGB video waveform of the SC7125. The influence of $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ on the analog video waveform is illustrated. Table 8 shows the detail of the resultant effect on the analog outputs of $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$. All digital inputs are TTL-compatible.

CLOCK INPUT

The CLOCK input of the SC7125 is typically the pixel clock rate of the system. The clock input is TTL-compatible. All video data and control inputs are registered into the SC7125 on the rising edge of CLOCK. It is recommended that the CLOCK input to the SC7125 be driven by a TTL buffer to avoid reflection induced jitter, overshoot, and undershoot.

RED AND BLUE		GREEN	
mA	V	mA	V
18.62	0.7	26.67	1.00
0	0	8.05	0.3
		0	0



NOTES
1.OUTPUTS CONNECTED TO A DOUBLE TERMINATED 75Ω LOAD.
2.VREF=1.235V,RSET=530Ω.
3.RS-343 LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

Figure13. RGB Video Output Waveform

Table8 . Video Output Truth Table (R_{SET} = 530Ω, R_L = 37.5Ω)

Video Output Level	IOG(mA)	$\overline{IOG}$(mA)	IOR/IOB(mA)	$\overline{IOR}$/$\overline{IOB}$(mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
White Level	26.67	0	18.62	0	1	1	0x3FFH
Video	Video+8.05	18.62-Video	Video	18.62-Video	1	1	Data
Video to $\overline{BLANK}$	Video	18.62-Video	Video	18.62-Video	0	1	Data
Black Level	8.05	18.62	0	18.62	1	1	0x000H
Black to $\overline{BLACK}$	0	18.62	0	18.62	0	1	0x000H
$\overline{BLANK}$ Level	8.05	18.62	0	18.62	1	0	0xXXXH
$\overline{SYNC}$ Level	0	18.62	0	18.62	0	0	0xXXXH

VIDEO SYNCHRONIZATION AND CONTROL

The SC7125 has a single composite sync ($\overline{SYNC}$) input control. When the $\overline{SYNC}$ input be tied to logic 1, the sync current is internally connected directly to the IOG output, thus encoding video synchronization information onto the green video channel. If it is not required to encode sync information onto the SC7125, the $\overline{SYNC}$ input should be tied to logic 0.

REFERENCE INPUT

The SC7125 contains a built-in 1.235V bandgap reference. The VREF pin is normally terminated to GND through a 0.1µF capacitor. Alternatively, if required, it can also be flexibly overdriven by an external 1.235V reference.

A resistor, R_{SET} connected between the R_{SET} pin and GND, determines the full range of the output current according to the Equation 1 and Equation 2 for the SC7125.

IOG (mA) = 11,445×VREF (V)/R_{SET} (Ω) (Eq.1)

IOR, IOB(mA)=7989.6×VREF(V)/R_{SET} (Ω) (Eq.2)

When $\overline{SYNC}$ is connected to Logic 1, Equation 1 applies to green channel, while Equation 2 applies to

red and blue channel. When $\overline{SYNC}$ is connected to Logic 0, Equation 2 applies to all the three channels.
Using a variable value of R_{SET} allows for accurate adjustment of the analog output video levels. The 530Ω resistor is suitable for most applications requiring 700-mV output level. These values typically correspond to the RS-343A video waveform values, as shown in Figure 13.

ANALOG OUTPUTS

The SC7125 has three differential analog outputs, corresponding to the red, green, and blue video signals. The three analog outputs of the SC7125 are high impedance current sources. Each one of these three current outputs can directly driving a 37.5Ω load, such as a doubly terminated 75Ω coaxial cable. Figure 14 shows the required configuration for each of the three RGB outputs connected into a doubly terminated 75Ω load. This arrangement develops RS-343A video output voltage levels across a 75Ω monitor. A suggested method of driving RS-170 video levels into a 75Ω monitor is shown in Figure 15. The output current levels of the DACs remain unchanged, but the source termination resistance, Z_S, on each of the three DACs is changed from 75Ω to 150Ω.

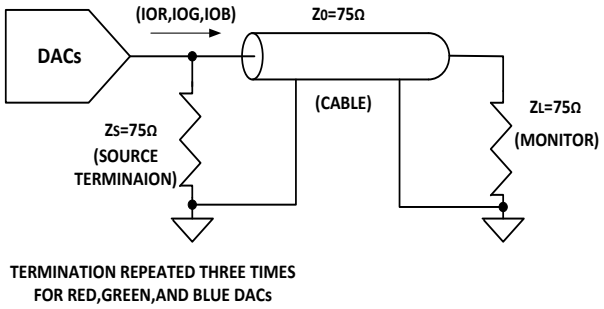


Figure14. Analog Output Termination for RS-343A

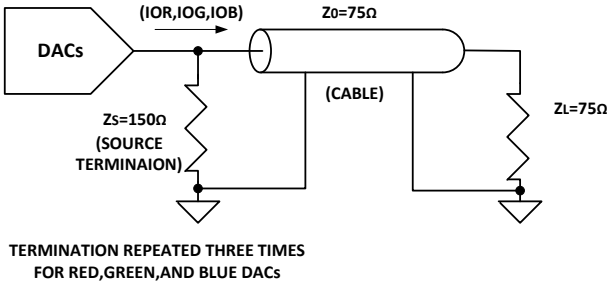


Figure15. Analog Output Termination for RS-170

Figure 13 shows the video waveforms associated with the three RGB outputs driving the doubly terminated 75Ω load of Figure 14. As well as the gray scale levels, black level to white level, Figure 13 also shows the contributions of $\overline{SYNC}$ and $\overline{BLANK}$ for the SC7125. These control inputs add appropriately weighted currents to the analog outputs, producing the specific output level requirements for video applications. Table 8 shows the detail of how the $\overline{SYNC}$ and $\overline{BLANK}$ inputs modify the output levels.
In some applications it may be required to drive long transmission line cable lengths. Cable lengths greater than 10 meters can attenuate and distort high frequency analog output pulses. So it is needed output buffers to compensate for some cable distortion. Buffers with large full power bandwidths and gains between two and four are required. These buffers also are required to supply sufficient current over the complete output voltage swing.

GRAY SCALE OPERATION

The SC7125 can also be used for standalone, gray scale (monochrome). Any one of the three channels, red, green, or blue, can be used as the input of the digital video data. The other two unused data channels should be tied to Logic 0. The unused analog outputs should be terminated with the same load as the one for the used channel. Such as, if the red channel is used and the output IOR is terminated with a doubly terminated 75Ω load (37.5Ω), IOB and IOG should be terminated with the same 37.5Ω resistors (see Figure 16).

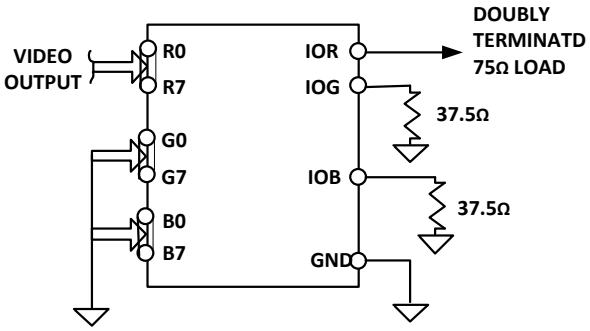


Figure16. Input and Output Connections for Standalone Gray Scale or Composite Video

POWER SAVE MODE OPERATION

The SC7125 may be powered down by tying the $\overline{PSAVE}$ pin to Logic 0. In this case, the supply current is reduced to less than 1mA typically. A built-in active pull-up circuit guarantees that the SC7125 remains enabled as this pin is left disconnected.

PCB LAYOUT CONSIDERATIONS

The SC7125 is optimally designed for the best noise performance, both radiated and conducted noise. To complement the excellent noise performance of the SC7125, it is imperative that great care be given to

the PCB layout. Figure 17 shows a recommended connection diagram for the SC7125.

Grounding and power-supply decoupling strongly influence the performance of the SC7125. Unwanted digital crosstalk may couple through the input, reference, power-supply, and ground connections, which may affect dynamic specifications like SNR or SFDR. The layout should be optimized for lowest noise on the SC7125 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. Shorten the lead length between groups of V_{AA} and GND pins to minimize inductive ringing. A multilayer PCB board with separate ground and power-supply planes is recommended. The ground and power planes should separate the signal trace layer and the solder side layer. Noise on the analog power plane can be further reduced by using multiple decoupling capacitors (see Figure 17). Optimum performance is achieved by using 0.1µF and 0.01µF ceramic capacitors. Individually decouple each V_{AA} pin to ground by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance. It is important to note that while the SC7125 contains circuitry to reject power supply noise, this rejection decreases with frequency. The power-supply voltages should also be decoupled at the point they enter the PCB board with large tantalum or electrolytic capacitors. Ferrite beads with additional decoupling capacitors forming a pi network could also improve performance.

Isolate the digital signal lines to the SC7125 as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane. Long clock lines to the SC7125 should be avoided to minimize noise pickup.

Place the SC7125 as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch. The video output signals should overlay the ground plane and not the analog power plane, thereby maximizing the high frequency power supply rejection. For optimum performance, each of the three analog outputs should have a 75Ω source termination resistance (doubly terminated 75Ω configurations) to ground. This termination resistance should be as close as possible to the SC7125 to minimize reflections.

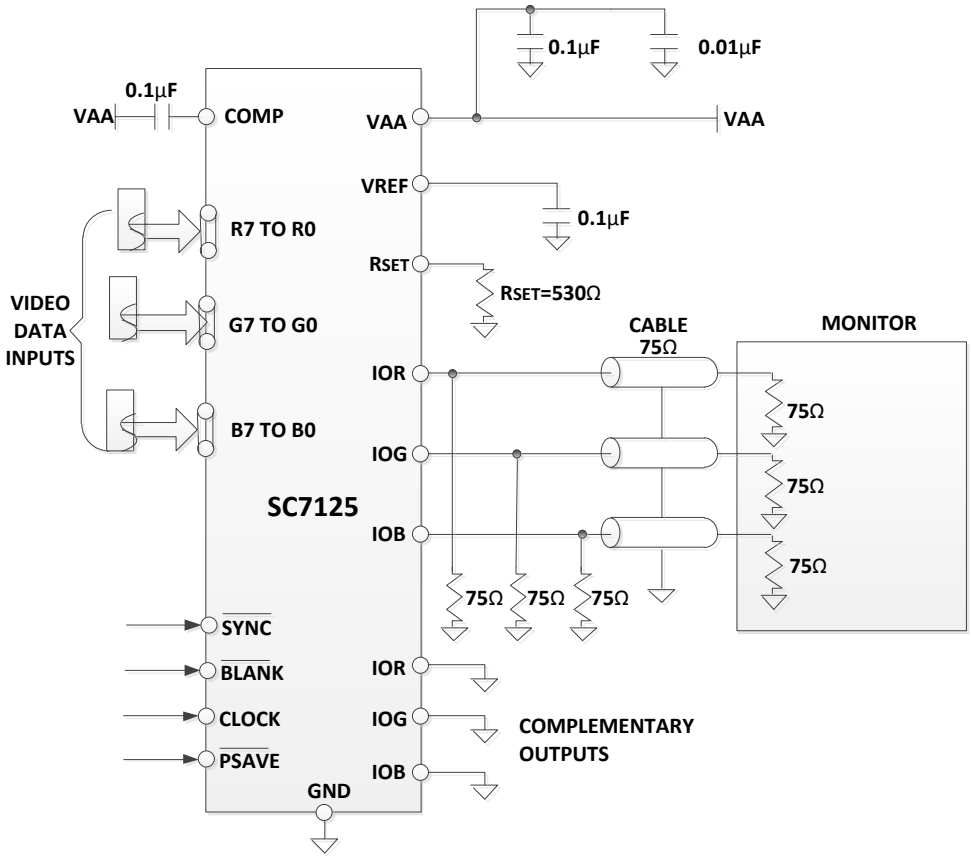


Figure17. Typical Connection Diagram

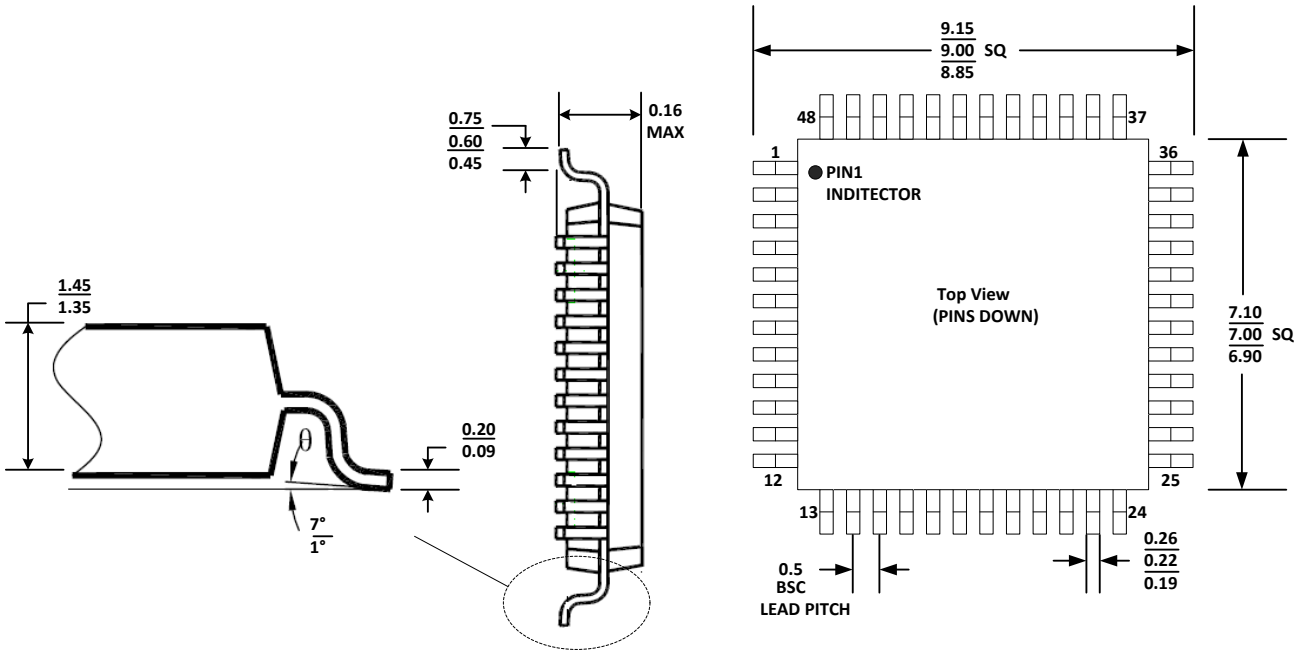


Figure 18. 48-Lead Low Profile Quad Flat Package [LQFP]
(Dimensions shown in millimeter)